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A GALLIUM ARSENIDE MESFET OPERATIONAL AMPLIFIER FOR USE IN COMPOSITE OPERATIONAL AMPLIFIERS

by

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Gallium Arsenide MESFET Operational Amplifier to be used

in Composite Operational Amplifier Design

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Abstract

A gallium arsenide (GaAs) MESFET operational amplifier for use in composite operational amplifier (CNOA) configurations is described. This device is guaranteed to be suitable for construction in CNOA models. The GaAs op amp design is a general-purpose device that exhibits a low-frequency gain of approximately 32dB and an open-loop unity gain frequency of 1.3GHz. The input offset voltage of the op amp is 20mV. These parameters are essential for optimum composite operational amplifier performance. Development and simulation of the GaAs op amp is presented.

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I. INTRODUCTION

The Operational Amplifier (op amp) is arguably the most powerful analog integrated circuit (IC) in the electronics industry. Its multiuse is unprecedented. Op amp applications can range from simple designs like those found in RC timers to more complex circuitry involved in high-speed switching, computer signal processing, and radars. Over the years, op amps have evolved and matured form the early days of huge vacuum tubes the size of breadboxes to microcomponents that can rest on the tip of a finger. Yet, these devices are not flawless. Its high unit gain frequency (f_t), at the cost of increased distortion, limited bandwidth, and low slew-rate are a few of the drawbacks resident to the op amp. This research will attempt to develop a general-purpose GaAs op amp that could adequately be used in composite operational amplifiers (CNOAs), with subsequent use in switched-capacitor filter networks.

Even though the application of GaAs technology in analog VLSI design is somewhat recent, it has been employed in digital and microwave systems since shortly after its discovery. GaAs MESFET technology first stepped onto the scene in the early 1970's. Early test data results were laboratory based only. Yet, its performance was very promising. The GaAs MESFET offers superior bandwidth and a high f_t as compared to its silicon competitor. It is for this characteristic that a GaAs MESFET device was chosen for development with future use in composite op amps.

Composite op amps were developed in 1981, and were designed to extend the operational bandwidth of a single op amp [1], [2], and [40]. This device is highly versatile. It guarantees increased bandwidth and slew rate over a single op amp. The generation of C2OAs is briefly discussed in Chapter IV. C2OA is one of many subcategories of CNOAs, incorporating two single op amps in the composite. C3OA, C4OA, etc. are also possible.

Limitations customarily associated with single op amp designs are significantly mitigated in C2OA configurations. Although, C2OAs will not be designed and simulated in this research, a background discussion is necessary to provide a framework in which to develop the GaAs op amp.

By incorporating GaAs technology, C2OA designs will lead to an op amp that possesses a substantial increase in bandwidth. They will have immediate application in switched-capacitor filters, analog converters, signal processing, and several other designs.

The following Chapters will provide greater insight concerning the topics just mentioned. GaAs MESFET physical properties, operation, and equivalent circuit models are presented in Chapter II. The actual GaAs op amp design is in Chapter III. Chapter IV discusses the various composite op amp topologies. Chapter V provides simulation results of the GaAs op amp. The final Chapter contains the study conclusions and recommendations for future research.

II. GALLIUM ARSENIDE (GaAs) MESFET DEVICES

A. General:

Gallium arsenide integrated circuit technology has evolved into an extremely viable choice for achieving high-speed and wide bandwidth in digital and analog circuits respectively. This compound semiconductor is formed from gallium and arsenic. It is duly noted for its high drift mobility (μ_n) and peak electron velocity as compared to silicon. This results in higher f_t in GaAs transistors than in comparable Si transistors [3] and [6].

While GaAs integrated circuit technology is somewhat new in analog VLSI applications, it has been used for a number of years in microwave and digital integrated circuits. As the cost of GaAs decreases its role in analog ICs will increase. Advances in GaAs ICs will provide inroads for improved switched-capacitor filters, A/D and D/A converters, and large-signal multipliers. Other applications that have benefitted from this technology include video processing, radar systems, ground based navigation systems, FDM telephone, data communications, etc.

This Chapter will focus on the physical properties of GaAs MESFET devices and some of the key parameters involved in the design of ICs. A brief discussion on level shifters using schottky-barrier diodes, differential amplifiers (diffamp), bootstrapping, current mirrors, and other circuit configurations will be presented. Also, some MOS equivalent circuit models and analog components will be presented. These techniques are vital in the development of GaAs operational amplifiers. In no way will this section attempt to cover all the known methods used in building GaAs MESFET ICs. Last, a discussion about the simulation software tool and its specific parameter values used in the research will be given.

B. Physical Properties of GaAs MESFETs:

1. Comparison Between MOSFET and MESFET Devices:

GaAs MESFETs offer improved high frequency performance over silicon MOSFETs. The two major differences between the devices are: (1) how the channel is formed and (2) how the gate-control electrode is coupled to the channel. First, the channel of the device is formed by GaAs or Si semiconductor material, based on the required application. Second, in a MOSFET, the gate-control electrode is separated from the channel by a thin oxide dielectric layer. Conversely, a MESFET uses a thin doped channel the thickness of which is controlled by the depletion of the metal semiconductor junction. Basically, the metal gate-control electrode is directly connected to the channel [3]. Figure 2.1 illustrates the two different types of gate structures for MOSFET and MESFET devices respectively.

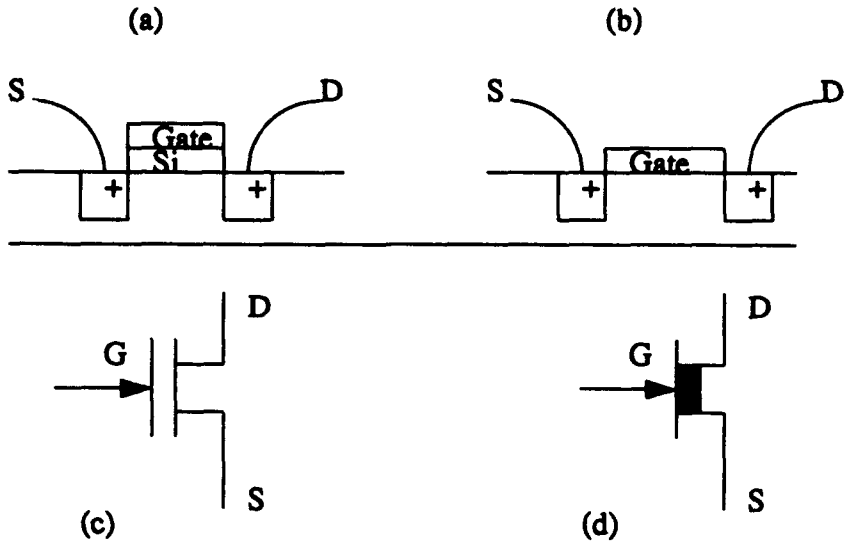


Fig. 2.1 n-channel cross-sectional areas of (a) MOSFET (b) MESFET and device symbols (c) MOSFET (d) MESFET

2. GaAs Physical Device Model:

Currently, n-channel GaAs devices are the most commonly available. The n-channel device has a much higher drift mobility then the p-channel, thus rendering the p-channel device less useful. Moreover, the physical design of the MESFET device is very similar to that of a MOSFET. Also, the analytical expressions used to describe a Si JFET can also be used with GaAs MESFETs. GaAs technology is built around two major elements, the Schottky-barrier diode (SBD) and the MESFET. The cross-section of a GaAs schottky-barrier diode and a MESFET are shown in Figure 2.2. The operation of these two

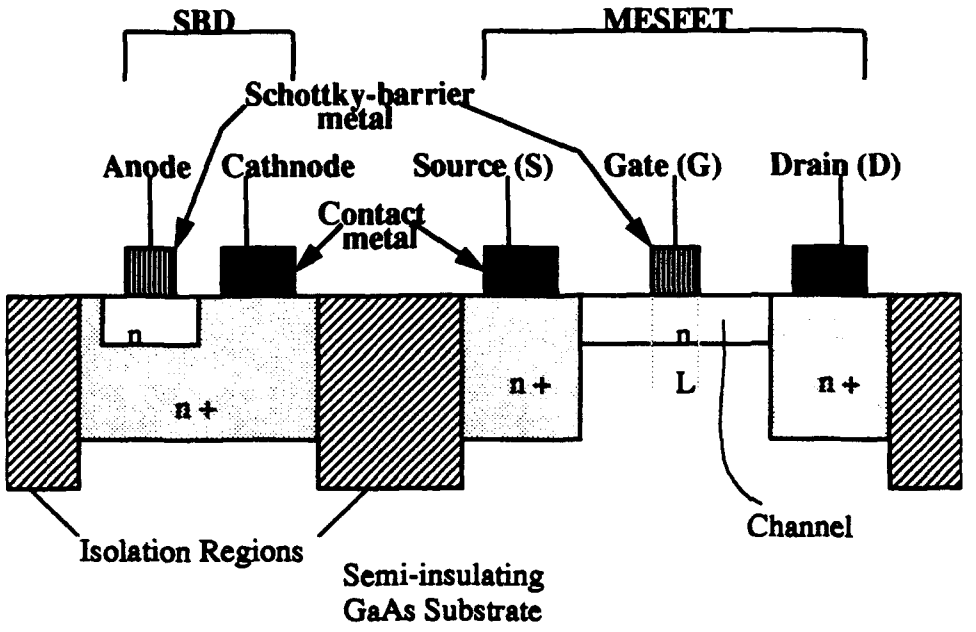


Fig. 2.2 Cross-section of a GaAs Schottky-barrier diode (SBD) and a MESFET [6]

key components will be covered later. The use of SBDs can assist with space conservation during Very Large Scale Integrated (VLSI) circuit layouts. The schottky barrier metal forms the anode end of the diode, and is identified as such to differentiate it from the n-type GaAs semiconductor that forms the cathnode. Additionally, the device is called semi-insulating because the chip is formed on an undoped GaAs substrate; and this substrate has a very low conductivity. This low conductivity property aids in isolating the devices on a chip from other components, and reduces stay capacitance effects [14]. The diagram above

provides an excellent cross-sectional view of how the MESFET and SBD elements are comprised. For a more extensive look at these elements see [3], [6], [14], [15], [16], and [17].

3. DC Design Concerns:

The major advantage a GaAs MESFET has over silicon is its much higher gain-bandwidth product (GBWP). However, a setback to the device is its dc characteristics as compared to silicon, such as gain. Low gain in GaAs MESFET causes low DC gain in GaAs op amps. Another problem often encountered in GaAs IC design is low frequency oscillation [30]. It is believed that a voltage applied across the semi-insulating GaAs material could cause a negative resistance which is responsible for the low frequency oscillations. Specific dc characteristic concerns germane to the operational amplifier used in this research are presented in sub-paragraph (d) of this Chapter.

The most fundamental difference between the MOSFET and MESFET device is the forward dc conduction limit of the MESFET at the gate-to-channel junction. Because of this dc conduction, the MESFET circuit is less robust in a noisy environment. Figure 2.3 depicts a MOSFET (NMOS) simple inverter device characteristics with a load resistor R_L

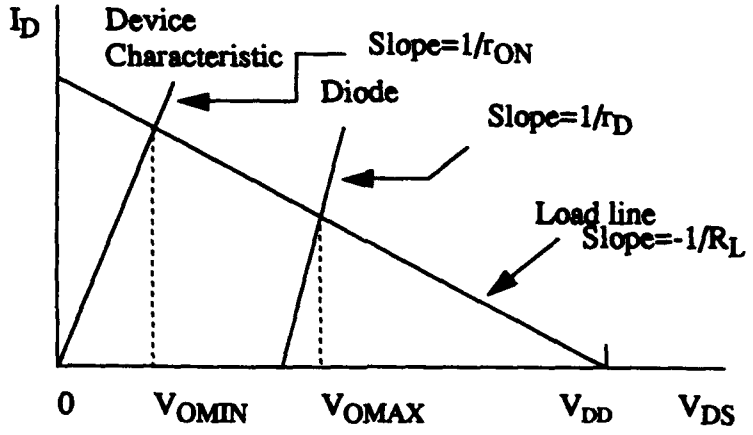


Fig. 2.3 Device characteristics of a simple inverter NMOS and MESFET equivalent circuit.

and a diode for a MESFET p-channel equivalent circuit model. Using the basic NMOS circuit model already developed makes it easier to design new circuit models for GaAS

MESFETs. Consider a simple inverter circuit with a NMOS switching transistor and a load R_L. When the switch is closed, the output voltage is in a minimum state (logic low level) and the output voltage minimum, $V_{O(MIN)}$ can be represented by the voltage divider equation:

$$V_{O(MIN)} = \frac{V_{DD} r_{ON}}{r_{ON} + R_L} \qquad \text{(EQ:2.1)}$$

Therefore, the value of $V_{O(MIN)}$ can be computed, given the necessary parameters. Now suppose the switch is open, the output voltage is in a maximum state (logic high level), and $V_{O(MAX)}$ is equal to V_{DD}. This occurs because the circuit responds to the effects brought on by the load resistor R_L. However, at no time will $V_{O(MAX)}$ exceed the value of V_{DD}. As seen from Figure 2.3, the load line characteristic curve with slope -1/ R_L, crosses the device characteristic curve whose slope is $1/r_{ON}$, (where r_{ON} is the transistor channel resistance) resulting in what was the minimum resistance output voltage increasing to the maximum resistance output voltage.

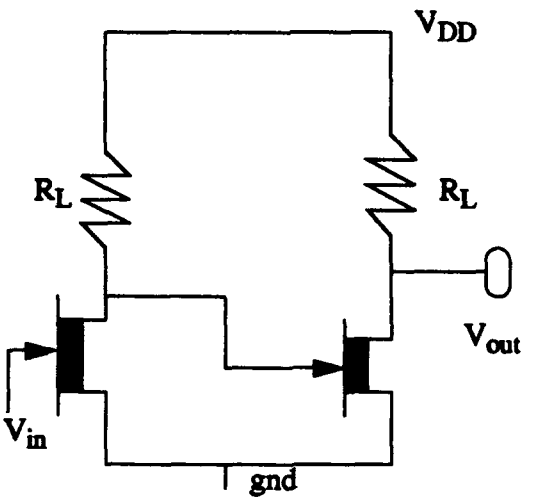


Fig. 2.4 MESFET inverter pair

In developing an equivalent MESFET circuit model from a MOSFET model using a simple inverter circuit, the diode in Figure 2.3 was needed. In MOSFET technology, the second stage would not require a dc conduction from the output of the first stage, see

Figure 2.4. However, the doped n-GaAs material composes the gate-to-channel junction and has a conduction limit of about 0.7 volts. The diode and its characteristic curve with slope $1/r_D$ (r_D = parasitic series resistance of the diode) are shown in Figure 2.3. This forward bias voltage is sufficient potential to turn the second stage transistor on. Accordingly, for GaAs when the output voltage is in its maximum state, $V_{O(MAX)}$ will never reach the value of V_{DD}. This reduction in $V_{O(MAX)}$ of a GaAs inverter is given by the intersection of the load line curve and the diode characteristic line. Thus, the reduced voltage experienced by the GaAs technology adversely affects its ability to properly operate in a noisy environment [3].

4. GaAs MESFET Frequency Analysis:

The primary reason GaAs MESFETs are used in analog ICs is to take advantage of their high f_t. To illustrate this inherent property and loading effects of the device, the equivalent circuit model Figure in 2.5 will be discussed. The transconductance parameter g_m depends inversely on the gate length and the depth of the gate-to-channel depletion layer. The gate length is controlled by design fabrication standards and the depletion layer depth is determined by the amount of doping in the channel. The depletion layer depth is reduced by increasing the channel doping. Consequently, this also increases the input capacitance C_{IN} in Figure 2.5. Depending on the design application, the trade-off between g_m and C_{IN} should be carefully considered. The resistance R_S is the parasitic resistance associated with the channel resistance r_{ON}.

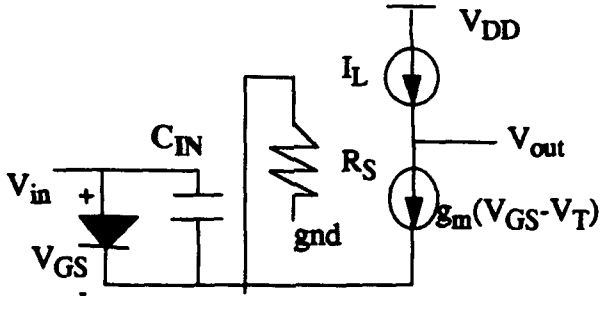


Fig. 2.5 Equivalent circuit model of inverter

The behavior of the MESFET dependent drain current I_D is a key performance parameter of FET IC design. Its characteristics can best be shown by using the curves in Figure 2.6. It is clear from the curves below that the drain current, with respect to the drain-

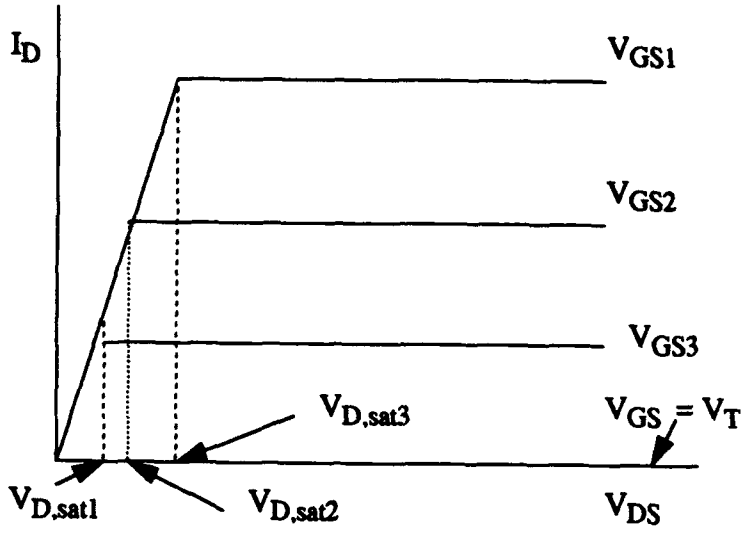


Fig. 2.6 MESFET drain current vs. drain-to-source voltage

to-source voltage, is nonlinear. The family of MESFET curves is generated by equally incrementing $V_{GS,}$ beginning at V_T as indicated in the Figure. $V_{D,Sat}$ represents the drain current saturation point for each curve. The effects of this saturation current is a function of the velocity of the electrons not increasing proportionally with the electric field in the channel. This effect also relates to the gate length adjustment shown on Figure 2.2. Therefore, the gate length plays a critical role in the amount of drain current in the device. Decreasing gate length and increasing the electric field in the channel will result in an earlier saturation drain current. So, in order to produce a small V_{DS}, a short gate length should be employed. The transconductance parameter scales inversly in MESFETs for long gate length ($L>5\mu m$), as previously mentioned. Usually, this capacitance is managed during the layout phase of the design. Increased capacitance can often be obtained by increasing layout capacitance between transistor stages. Additionally, a short gate length is advantageous to increasing device transconductance and reducing input capacitance (C_{IN}). This will be explained in further detail in the GaAs FET operation paragraph. Lastly, the

gate length and width of the device are two critical design parameters in the fabrication of GaAs integrated circuit technology.

5. GaAs FET Operation:

Now to explore how the device works and some of the analytical equations that are associated with its operation. The MESFET operates somewhat like the Si JFET device and many of the expressions used to describe the JFET are applicable to the MESFET, so long as no design properties are ignored. In a MESFET, a depletion region forms under the gate contact surface and the rate and depth of this depletion area is determined by the gate-to source voltage V_{GS}. The depletion in the channel changes the dimensions of the channel, and the current that flows from drain to source for some applied ac voltage v_{DS}. Moreover, it is through this ac drain-to-source voltage that abating occurs at the drain end, which ultimately results in pinch-off.

Currently, depletion mode GaAs MESFETs are the most used devices in industry. The circuit symbol for an n-channel depletion-type GaAs MESFET is shown at Figure 2.7. The arrow on the device will always point inward, since p-channel devices aren't used. The threshold voltage for these devices typically range from -0.4 to -4.0. MESFETs normally operate with a v_{GS} from negative V_t to a small positive voltage not to exceed the breakdown schottky-barrier voltage at the gate-to-channel junction, which is roughly 0.7 volts. Once the gate-to-source voltage approaches the barrier breakdown voltage, gate conduction occurs. Recall from earlier discussion that gate conduction does not take place in a MOSFET. Gate conduction in a MESFET is a considerable drawback in the operation of GaAs devices. Once gate conduction occurs, the gate-to-source voltage no longer controls the critical drain-to-source current I_{DS}. For this research, depletion type devices were used to design the GaAs amplifier.

Even though enhancement mode MESFETs are not used in this research, some are available. The enhancement MESFET has a threshold voltage between 0. 1 and 0.3. Refer to [8] for a more detailed study on enhancement MESFETs.

In [31] it was manifested that equation 2.2 is a valid drain current-to-gate voltage relationship for long gate length MESFETs without being greatly influenced by the doping quantity:

$$I_{D,Sat} = \beta (V_{GS} - V_T)^2 \qquad \text{(EQ:2.2)}$$

The parameter β is the transconductance parameter of the FET. An analytical expression for β, [32] is given in equation 2.3.

$$\beta = \frac{2\varepsilon_s \mu_n v_{sat} W}{b(\mu_n V_{po} + 3 v_{sat} L)} \qquad \text{(EQ:2.3)}$$

This is an excellent expression to illustrate the relationship of the drain current I_D and other key design parameters of the device. It shows how the drain current depends on both the drift mobility and saturated drift velocity. Furthermore, the equation indicates that the width and length can improve the current by selecting the appropriate values for each. Note, that for long L, equation 2.3 reduces to 1/L. Now, for shorter gate length, the current increases less rapidly than the ratio 1/L as the gate length is reduced. Also, adjusting the width and length of the MESFET is a common practice used by IC designers to improve device performance. The necessary models and equations needed to execute a program are often already included in the circuit simulation software tool (HSPICE was used in this research). More on MESFET width and length adjustment in Chapter III. V_{po} is the pinch-off voltage, and the reader should refer to [32] for information on ε_s and b.

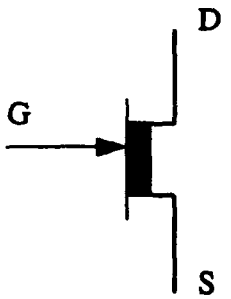


Fig. 2.7 n-channel depletion type GaAs MESFET symbol

Ignoring the velocity saturation effects of a first order MESFET will allow the use of JFET equations with only minor errors. These are basic JFET expressions and can be found in a general textbook on electronic integrated circuits.

The ac small-signal model for a MESFET is the same as for any JFET. Two of the essential ac parameters are g_m and r_o. They are determined as shown below:

$$g_m = 2\beta (V_{GS} - V_t)\ (1 + \lambda V_{DS}) \qquad \text{(EQ:2.4)}$$

$$r_o = \frac{1}{\lambda\beta (V_{GS} - V_t)^2} \qquad \text{(EQ:2.5)}$$

In a MESFET, the value λ ranges from 0.1 to 0.3 V^{-1}, which results in a small r_o component. The low small-signal model output resistance adversely affects the operation of the device. This ultimately causes a low voltage gain at each stage. Methods to increase the r_o value are contained in paragraph c. This is a major limiting factor in GaAs op amps, and limits open-loop gain.

6. Device Gain and Unity Bandwidth:

The greatest advantage a GaAs MESFET has over a silicon MOSFET is its much higher f_t. But, the resulting low open-loop gain in a GaAs op amp is a drawback. An extremely important ac parameter of the MESFET is transconductance g_m. It plays a significant role in the amount of open-loop ac voltage gain obtainable. Transconductance is defined as follows:

$$g_m = \left[\frac{\partial I_D}{\partial V_{GS}}\right]_{V_{DS} = constant} \qquad \text{(EQ:2.6)}$$

It is obvious from the expression above that the transconductance varies as a differential change in the ratio of I_D to V_{GS} for a constant V_{DS}. As such, it is closely related to the gain of a device. Now to explore the effects of g_m in a circuit application. A basic

single-stage amplifier will be examined, as pictured in Figure 2.8. Note that the circuit uses

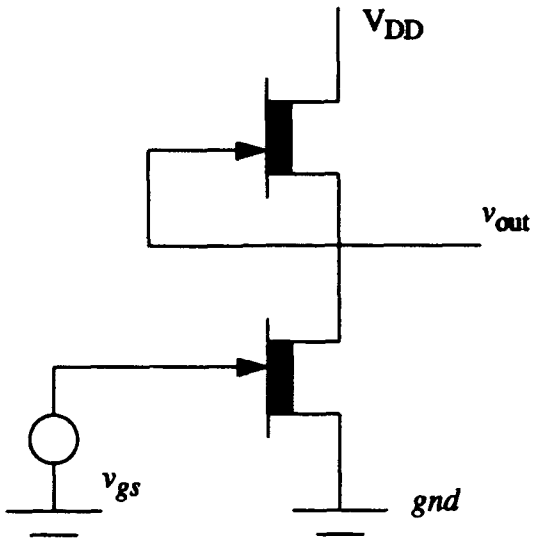


Fig 2.8 Single-stage active load GaAs amplifier

an active load in place of a resistor. The active load configuration is commonly used in IC design. Because it is easier to control the characteristics of a MESFET than the characteristics of a resistor. The resistor load would occupy more real estate on a chip as compared to an active load transistor. The load transistor is a depletion-mode MESFET with V_{GS}=0. Thus, higher gains can be achieved by providing sufficient supply voltage to maintain the active load device in the saturation region. This technique is employed quite extensively in MESFET ICs and is presented again in the amplifier design techniques paragraph. An ac analysis for the voltage gain A_v of Figure 2.8 is given as:

$$A_v = \frac{V_{out}}{V_{gs}} = -g_m R_L \qquad \text{(EQ:2.7)}$$

Here, the ac voltage open-loop gain is a function of the transconductance component of the device and the load resistor. However, a more useful expression for g_m of a MESFET is one that includes the drain current limit caused by velocity saturation. In [3] such a relationship for g_m is given by:

$$g_m = \frac{\varepsilon_s v_{sat} W}{d} \qquad \text{(EQ:2.8)}$$

where d is the doping distribution of N-type material in the channel of the device, and g_m varies inversely with d. Hence, to increase the value of g_m, the doping distribution must be reduced. To accomplish this requires increasing the channel doping. Observe that g_m depends inversely on the gate length L.

The transconductance parameter is vital to increased voltage gain but is not the only parameter affecting the frequency response. Therefore, the MESFET frequency response is better described by the unity gain frequency (f_t). This is measured by short circuiting the output of the high-frequency small-signal model of the FET. The unity gain frequency is expressed as:

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \qquad \text{(EQ:2.9)}$$

From this relationship it shows that the unity gain frequency is directly dependent on the transconductance. Thereby, increasing g_m has a positive effect on the bandwidth of the FET. Also, small-signal model gate capacitances Cgs and C_{gd} are a function of the gate-to-source and the gate-to-drain voltages. These capacitances should be minimized to improve the frequency response. An expression for f_t in terms of the gate length is more practical and desirable. Equation 2.10 (see [8] for derivation) below is more concise and useful:

$$f_t = \frac{v_{sat}}{2\pi L} \qquad \text{(EQ:2.10)}$$

This equation is used to estimate the unity frequency in the amplifier design stage and it compares favorably with already fabricated and tested ICs. Moreover, f_t varies inversely proportional to the gate length L. This will remain true so long as the gate capacitances maintain a direct relationship with the gate length. This effect can be disrupted by the fringing capacitance [33] which is caused by horizontally expanding the depletion

layer in the direction of the gate metal. Thus, to obtain maximum gain g_m through reduction of gate length, it would require sophisticated fabrication technology and controlling doping in the channel so that the ratio of fringing capacitance to plate capacitance stays modestly small. Besides, the added gain would be negligible as compared to the corresponding increase in bandwidth. Accordingly, a cost-efficiency trade-off analysis may prove beneficial. The GaAs amplifier analyzed and presented in Chapter III was simulated with a minimum gate length of 0.8μm. This is the smallest length the fabricator could reliably produce.

C. GaAs Design Techniques:

In this section, a few GaAs circuit design techniques and models associated with the construction of MESFET amplifier ICs will be presented. Also, a general purpose GaAs amplifier with reasonable gain (40dB) is offered. In addition, a method frequently used to overcome the low output resistance r_o in FETs when in saturation is given. Techniques discussed will focus mostly on the specific circuit design of the amplifier used in Chapter III; nevertheless, others will be outlined. This section is not intended to be all inclusive of the techniques and models that have been developed in recent years. However, other sources addressing and expanding on this topic are found in [3], [4], [8], and [10].

1. Schottky-Barrier Diodes and Level Shifters:

Both the schottky-barrier diodes (SBD) and voltage level shifter (V_{LS}) are key elements in GaAs MESFET IC applications. The schottky-barrier diode is a special type of diode that is formed from carefully doped n-type material. Figure 2.9 provides an excellent cross-sectional look at the schottky diode composition. As stated in previous sections, the schottky metal rests on the depletion layer (anode) and the ohmic contact to form the cathnode.

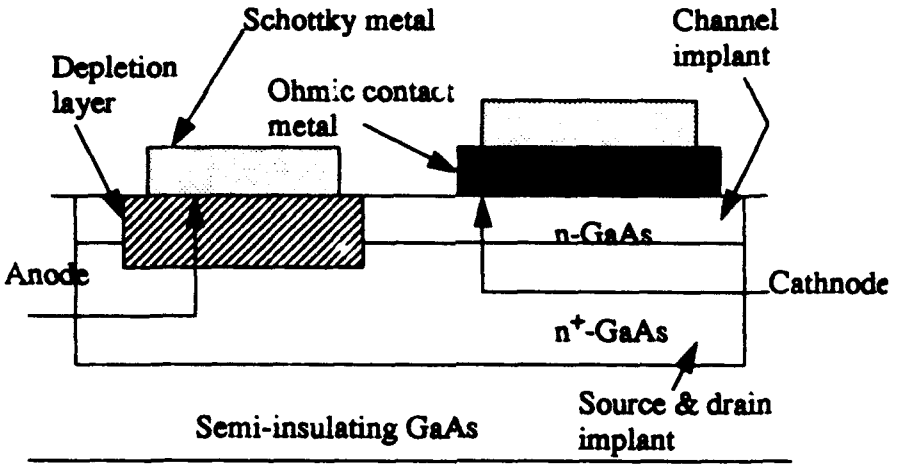


Fig 2.9 cross-sectional of schottky-barrier diode

A current-voltage characteristic curve of the schottky diode appears nearly the same as the pn-junction diode. The current flow of the schottky diode device is significantly different from the pn-junction diode in that the majority carriers (electrons) allow the conduction current and reverse saturation current. As a result, there is no large collection of minority carriers (holes) in the bulk region at doping amounts above a prescribe level. Since the diffusion capacitance in schottky diodes is negligible, it results in much faster transition time from forward bias to reverse bias as compared to the pn-junction diode. Because of these properties, the SBD is also identified as a majority carrier device. A properly n-type doped schottky metal has a voltage breakdown between 0.60 and 0.70volts, depending on the concentration of n-type doping. Therefore, significant forward bias current flow will occur after voltage breakdown. Continuing, the SBD's current-voltage characteristic curve is identical to the ideal diode I-V curve, and is given by:

$$I_D = I_S\left[exp\left(\frac{qV_{D,i}}{nkT}\right) - 1\right] \qquad \text{(EQ:2.11)}$$

I_S in this expression is the diode saturation current, n is the ideality factor or the emission coefficient. The variables q, k and T are charge, Boltzmann's constant, and

temperature in Kelvin respectively. The $V_{D,i}$ parameter is the intrinsic diode voltage that is present across the junction and is defined below:

$$V_{D,i} = V_D - I_D R_S \qquad \text{(EQ:2.12)}$$

where R_S is the series resistance due to contacts, neutral n-GaAs, and current crowding at the edges of the contacts. The series resistance is a by-product of how the diode is fabricated on a chip. The voltage gain g_m of the device (at each stage) and bandwidth could suffer [35] from excessive current crowding. Additionally, for simulation and design purposes, the series resistance is a constant ranging from 800Ω to 1500Ω (depending on the simulation tool used). Meticulous environmental control and detailed circuit layouts are just some of the ways to reduce series resistance (R_S) and current crowding. Lastly, V_D is the voltage at the diode leads.

The schottky-barrier diode is an integral element of GaAs MESFET design and simulation. For the GaAs amplifier design in Chapter III, the Vitesse simulation parameters and diode models for the SBD were used. In [3], [8], and [35] are descriptive analysis and simulation models of the SBD. Relevant to this research are the default and actual values used in the SBD design. These parameter values are shown in the Table below:

TABLE 2.1: Parameter values used in HSPICE for GaAs schottky diode model with a 1μm length and 1μm width [43]

Name	Parameter	Units	Default value	Actual value	Area
is	Saturation current	A	1.0e-14	10f	*
rs	Ohmic resistance	Ω	200	1500	*
n	Ideality factor	-	1.0	1.18	
tt	transit time	s	0	0	

TABLE 2.1: Parameter values used in HSPICE for GaAs schottky diode model with a 1μm length and 1μm width [43]

Name	Parameter	Units	Default value	Actual value	Area
cjo	Zero-bias junction capacitance	F	0	2.0e-15	*
vj	Built-in potential	V	1	0.8	
m	Grading coefficient	-	0.5	0.5	
r_d	Drain resistance	Ω	500	3K	
r_s	Source resistance	Ω	500	3K	

The asterisk (*) above indicates that the parameter is to be scaled with respect to the diode area. The scaled factor is usually defined in the model line and is intended to provide the designer greater flexibility in obtaining optimum circuit performance. For most software simulation tools the SBD's length (1μm to 3μm) is preset and the area of the SBD is determined by scaling the width parameter. Schottky-barrier diodes are constructed by connecting together the drain and source terminals of a MESFET transistor.

Some of the Vitesse diode parameter values are slightly different from other SPICE models. For instance, the SBD forward voltage drop can be varied by changing the scaling factor of the diode. As stated earlier, the drop can vary from 0.60 volts to 0.70 volts. It is customary for different foundries to use parameter values that closely fit their device characteristics.

The SBD is used in GaAs MESFET technology to provide a logic-switching element in digital systems and as a dc voltage level-shifter in analog integrated circuit designs. One of the earliest application of dc voltage level-switching networks in analog GaAs MESFET IC can be studied in [10]. As a level-shifter, the dc bias voltage allows for

the voltage potential at different nodes in the circuit to be controlled. A level-shifter is used with the amplifier designed in Chapter III. A typical level-shifter is shown at Figure 2.10. The level-shifter below is constructed of three equally sized SBDs. The effects the level-shifter has on the circuit will depend on the number of SBDs implemented in the diode series string, along with the length and width dimensions of the diodes.

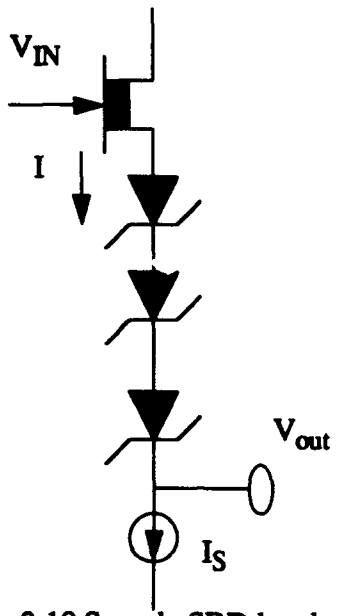


Fig. 2.10 Sample SBD level-shifter

2. Current Mirrors:

Another essential high-performance component of the GaAs MESFET analog ICs is the current mirror network. Current mirrors are added to integrated circuits to provide high resistance loads, current sources, and level shifters. Probably the greatest benefit of the current mirror is its increased output resistance which ultimately leads to higher output voltage if used as a load, and great current stability if used as a current source. A simple GaAs MESFET current mirror circuit is drawn at Figure 2.11 below:

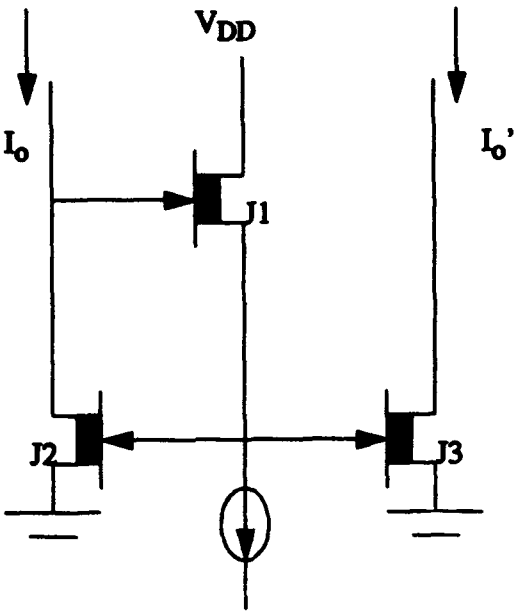


Fig. 2.11 GaAs MESFET current mirror [10]

The current mirror design above can be modified to include SBDs to reduce the dc voltage potential at certain nodes. Also, dc bias voltages (batteries) can be inserted to boost the voltage at desired nodes. Of paramount importance to the current mirror's performance is to ensure that the physical size (gate length and width) and the molecular composition of transistors J2 and J3 are nearly identical. A very similar current mirror design to the one above is presented in [10].

3. Small-Signal $g_m r_{ds}$ Effect:

GaAs MESFET technology suffers from low transistor $g_m r_{ds}$ which results from varying drain resistance r_{ds} at low-frequency [36] and [37]. The resistance value tends to be more stable (or constant) at around 1MHz and above. A small-signal equivalent circuit model will be used to illustrate the changing R_{DS} values and its adverse effect on the

system's performance. A signal analysis of Figure 2.12 below will reveal a voltage gain given by equation 2.13:

$$\frac{v_d}{v_{gs}} = -g_m(R_D \| r_o) \qquad \text{(EQ:2.13)}$$

where the negative sign indicates that the output signal at v_d (the drain terminal) is 180^0 out of phase with the input signal v_{gs}. Another salient point about equation 2.13 is that as r_o becomes small and g_m remains large, the value R_D will become negligible. Thus, equation 2.14 shows the new relationship that can be derived from Figure 2.12

$$Av = -g_m r_o \qquad \text{(EQ:2.14)}$$

A general expression and explanation of r_o can be found in [6]. A generic small-signal equivalent GaAs MESFET model is shown:

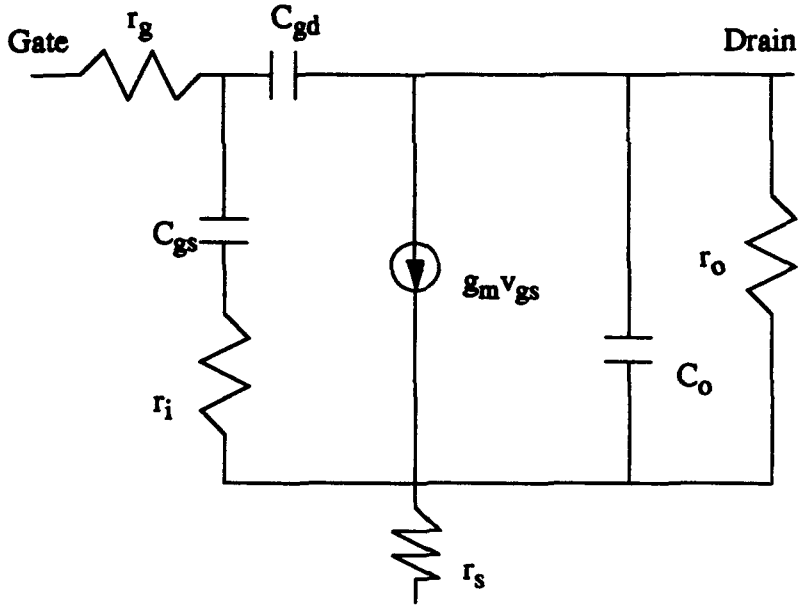


Fig. 2.12 Typical small-signal equivalent GaAs MESFET model [9]

Carefully treating (w/ molecular beam epitaxy) and constructing the active channel layer of the depletion-mode N-channel device will significantly enhance insulating properties and low-frequency $g_m r_{ds}$ and reduce backgating and light sensitivity [9]. An

acceptable value for the resistance R_{ds} should be strictly monitored and obtained at each stage. For MESFET technology, the output resistance ought to be around 20Ω. Achieving this resistance is a 'tricky' and challenging procedure for analog circuit designers. Figure 2.13 represents the varying drain resistance as a function of frequency.

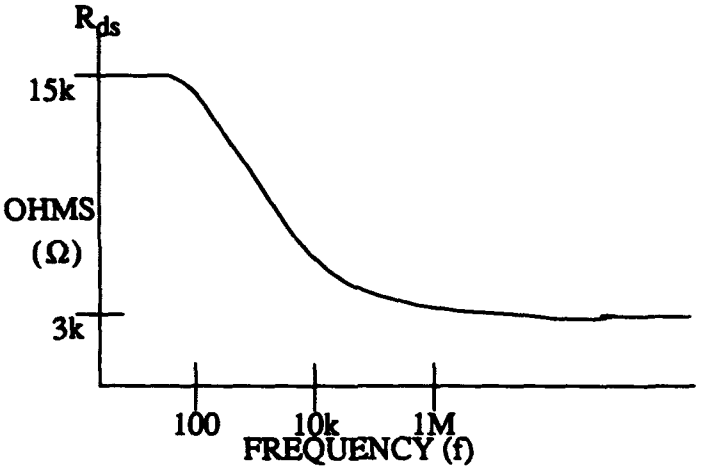


Fig. 2.13 MESFET output resistance vs. frequency [10]

The curve clearly shows the degree of variance of the value R_{ds} at low-frequency, and that the resistance settles to a constant value at approximately 1MHz. This behavior of the MESFET drain resistance is also reported in [9], [10], [38], and [39]. Better environmental control measures and elaborate modelling techniques have significantly raised the value of $g_m r_{ds}$. In recent years, several methods have been developed to improve or eliminate the undesirable effects of varying drain resistance at low-frequency, backgating, and low-light sensitivity [9], and [17].

4. Gain Enhancement Techniques:

This section covers techniques often used to improve FET gain and overall FET performance in IC designs. Many of the models and configurations presented were originally developed for MOSFET applications but have been adapted for GaAs MESFET IC technology.

a. GaAs Differential Amplifier Pair:

The differential amplifier stage is the fundamental building block of analog VLSI design and operational amplifiers. Differential amplifiers are frequently used in comparators, multivibrators, logic gates, operational amplifiers, A/D converters, etc. Currently, there are several GaAs MESFET differential amplifier topologies available. References [3], [6], [9], and [10] provide instructional techniques for the construction of such amplifiers. In Figure 2.14, a general purpose depletion mode GaAs MESFET differential amplifier is shown. Design considerations for a high performance and high

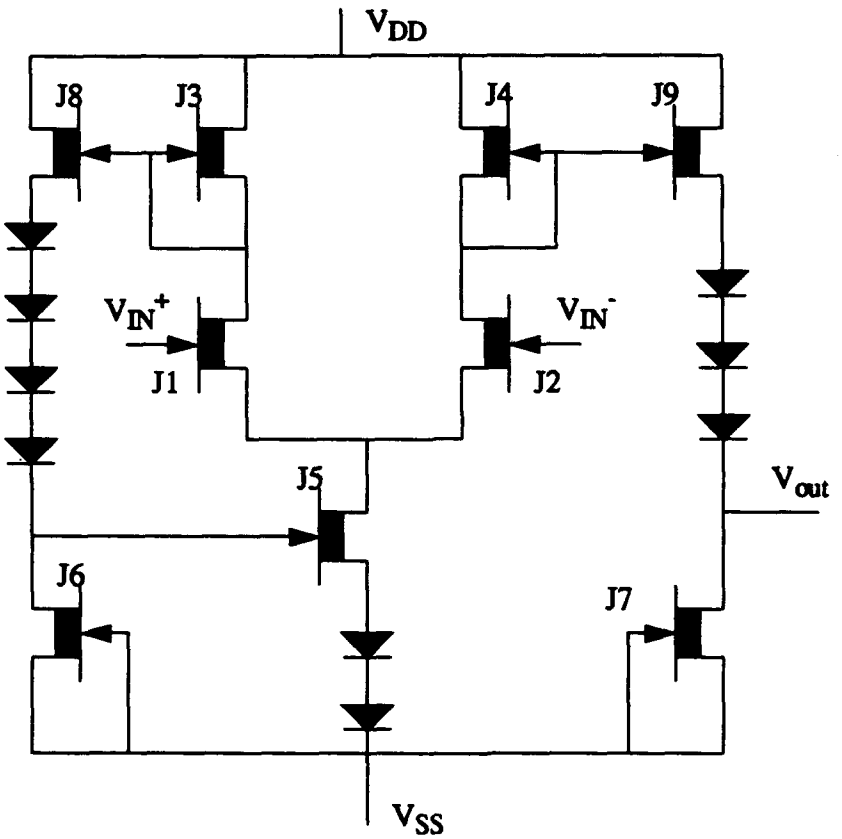


Fig. 2.14 Depletion-mode GaAs Differential Amplifier [40]

yield differential amplifier stage must include bandwidth, common-mode range, common-mode rejection, and input-offset voltage requirements. This particular differential amplifier has exhibited a gain bandwidth product of approximately 4MHz and an average gain of 22dB under typical IC applications. Explicit design techniques and methodology

concerning this amplifier is contained in [4], [6], [12], and [40]. The topology used in the amplifier design of Chapter III is very similar to the one in Figure 2.14 above.

b. Current Source Model:

The current source is one of the most basic designs of integrated-circuits, providing both active loads and biasing requirements. Improved amplifier gain can be accomplished by appropriately adjusting the gate length and width. The current source circuit can be employed by connecting the gate terminal of the depletion-mode MESFET to the source terminal. So long as v_{DS} is kept above $|V_t|$, the MESFET will operate in the saturation region and the standard expression for i_D is applicable. A current source and its equivalent circuit design are shown in Figure 2.15 below:

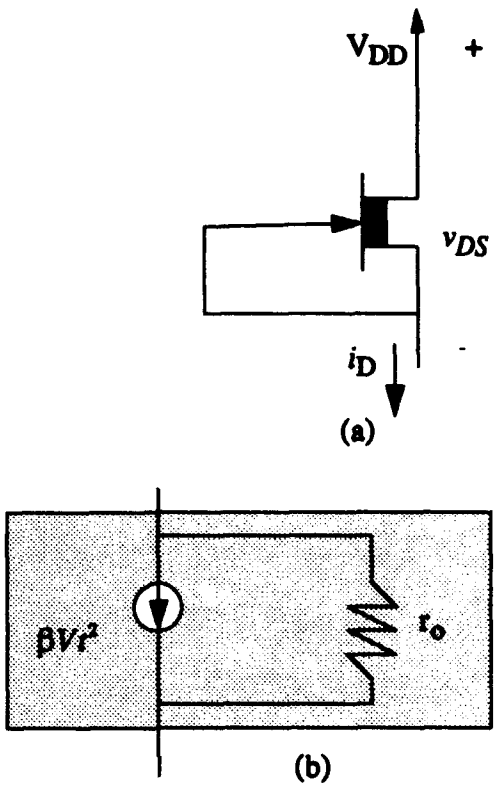


Fig. 2.15 (a) MESFET current source connected to positive power supply; (b) equivalent circuit of current source

Refer to previous discussions and references concerning the relationship for r_o and i_D in the network above. In most IC applications, the gate width of the current source is reasonably small, as compared to the gate width of the source follower.

c. GaAs Cascode Current Source:

The cascode current source model is a design used primarily to increase the output resistance R_o of the current source circuit. The effects of incorporating a second transistor to the current source is define by:

$$R_o = g_{m2} r_{02} r_{01} \qquad \text{(EQ:2.15)}$$

A simple circuit analysis of Figure 2.16 shows the output resistance of the current source component of J1 is scaled by $g_{m2}r_{02}$, the small-signal gain of J2. Typically, the scale

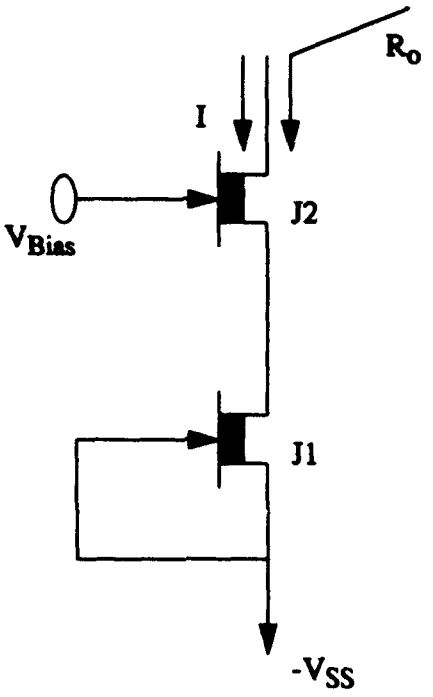


Fig. 2.16 GaAs cascode current source

value ranges from 20 -50 in GaAs devices. Additionally, a design requirement for V_{Bias} is for the voltage potential to be the smallest possible that will maintain the saturation operation of J2. This will allow for a larger voltage range at the output of the cascode current source. This technique is frequently employed in GaAs MESFET integrated circuit designs [11] to boost the voltage gain.

d. Bootstrapping Current Source:

Much like the cascode current source, the MESFET bootstrapping current source is another circuit often used to increase the output resistance of a current source. However, the complexity of the circuit implementation and its design makes it a less attractive model. The major idea behind this method is to induce an incremental voltage at the node of the current source A in Figure 2.17, which will cause a corresponding

incremental voltage change at the output node B. These two voltages are related by an

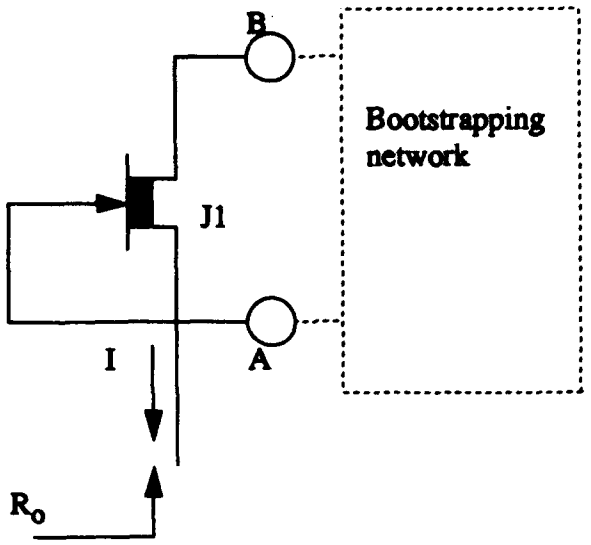


Fig. 2.17 Basic circuit configuration for a GaAs MESFET bootstrapping current source [6]

incremental change factor α, where α is a constant ≤ 1. Therefore, the output resistance R_o is determined by a straightforward circuit analysis of Figure 2.17, resulting in:

$$R_o = \frac{r_o}{1-\alpha} \qquad \text{(EQ:2.16)}$$

Clearly, from equation 2.16, the output resistance is scaled by the factor $\frac{1}{1-\alpha}$.

The output resistance would increase as α approaches 1. Also, maximum bootstrapping occurs when $\alpha = 1$, leading to $R_o=\infty$. Finally, a greater amplification of the GaAs bootsrtapping current source and derivation for the parameter α can be found at [6]; and a design application at [11].

D. GaAs Device Design Parameters:

All GaAs MESFET models and equations must operate at an acceptable accuracy. It is critical for the MESFET models to work effectively, as there may be many other elements and subcircuits comprising the network. There are several simulation software

tools available, each with slightly different design parameter values. HSPICE was the simulation software used to simulate the amplifier of Chapter III. HSPICE is extremely accurate, and provides an excellent Graphical Simulation Interface (GSI) module. The GSI tool renders the simulation output under a separate file catalog, making it easier for the user to view, update the file, and to print necessary results. See references [3] and [8] for other design models and simulation tools.

Additionally, HSPICE employs the Vitesse corporation gallium arsenide MESFET design models and parameter values. The construction of both the GaAs schottky-barrier diode and transistor were previously discussed. Furthermore, changes to the Vitesse model, parameter values, and creation of new parameter values were prohibited, due to future design layout and fabrication requirements. That is, the only user design parameter flexibility allowed was to alter the devices gate length and width. The Vitesse MESFET model parameters are shown below for the gate capacitance and DC model, and the temperature effect parameters in Tables 2.3 and 2.4 respectively.

TABLE 2.2: Gate Capacitance and DC Model Parameters

Name	Parameter	Unit	Vitesse	Default
CAPOP	Cap. option	F	1.0	0
CGAMDS	Threshold lowering factor cap	F	0.065	0
CRAT	Source fraction gate cap.	F	0.666	0.666
GCAP	Zero-bias gate cap.	F	1.7e-3	
BETA	Gain	amp/V^2	1.9e-4	1.0e-4
LAMBDA	Channel length mod.	1/V	0.065	0

TABLE 2.2: Gate Capacitance and DC Model Parameters

Name	Parameter	Unit	Vitesse	Default
VTO	Threshold voltage	V	-0.825	-2.0
LEVEL	FET level	n:	3	3
ALPHA	Sat. factor	1/V	3.5	2.0
D	Dielectric constant		Si=11.7 GaAs=10.9	11.7
K1	Threshold voltage sens	V^2	0.350	0
ND	Drain fact	1/V	0.2	0
NG	Gate fact.		1.1	0
SAT	Sat. factor		3	0
SATEXP	Drain voltage exp.		3	3
UCRIT	Critical field	V/cm	0.5	0
VGEXP(Q)	Gate exp.		2	2

TABLE 2.3Temperature Effect Parameters

Name	Parameter	Unit	Vitesse	Default
BEX	Mobility temp coeff.		-0.4	0
EG	Energy gap	ev	Si=1.17 SBD=0.69 Ge=0.67 GaAs=1.52	1.16
GAP1	1st bandgap	ev/deg	Si=4.73e-4 Ge=4.56e-4 GaAs=5.41 e-4	7.02e-4

TABLE 2.3Temperature Effect Parameters

Name	Parameter	Unit	Vitesse	Default
GAP2	2d bandgap	deg	Si=636 Ge=210 GaAs=204	1108
TCV	Temp comp coeff VTO	1/deg	1.10e-3	0
TLEV	Temp eqn		2	0
TRD	Temp coeff drain resist	1/deg	3.3e-4	0
TRS	Temp coef source resist	1/deg	3.3e-4	0
XTI	Sat current temp exp		2	0

The gate length (L) and width (W) parameters for the device are fixed in the algorithm so that L and W vary between the ranges $0.4 \leq L \leq 1.2499\mu m$ and $0.5 \leq W \leq 10000\mu m$. In order to obtain a different L and W range, a new Vitesse model number must be selected. HSPICE has three Vitesse GaAs transistor devices of semi-fixed lengths 1,2, and $3\mu m$. Vitesse also provides enhancement and depletion-mode MESFETs at the gate lengths already mentioned. The parameter values listed in Tables 2.1, 2.2, and 2.3 were obtained from the hgaas3.model, depletion-mode 1.1 (dp1.1) of the Vitesse library. Specific equation derivations and relationships can be found in reference [43] Meta Software.

III. GaAs MESFET OPERATIONAL AMPLIFIER DESIGN

A. General:

The operational amplifier (op amp) is an essential and reliable component in the electronic technology industry. Op amps were first introduced in the late 1940s. The single vacuum-tube op amp, invented by G. Philbrick [5], was one of the first op amp circuits published. These initial op amps were extremely large (in size), expensive, and performed only simple mathematical computations.

It wasn't until almost two decades later that solid-state technology (transistors) made their way onto the scene. In the mid-to-late 60's, Fairchild perfected the now famous LM-741 integrated circuit op amp. This breakthrough in the electronics industry lead to remarkable strides in the computer and engineering sciences. The solid-state integrated circuit technology had taken root by the mid 70's, and new advancements in the field were rapidly coming to fruition. Additionally, the op amp was exceedingly more robust than its predecessor. It was physically smaller, less expensive, easier to work with, and far more capable than vacuum tube op amps.

The IC op amp became a major building block for more complicated designs. Engineers were able to get away from the rudimentary tasks of designing multiple discrete component subcircuits to achieve a particular performance level. A new and more powerful circuit (chip) can be designed from just an op amp, a few capacitors, and resistors. Today, op amps are readily available in a wide range of specifications, applications, and physical properties. The op amp is very simple to use and it operates closely to its ideal characteristics.

This Chapter will mainly focus on the GaAs MESFET operational amplifier design. A step-by-step design and a completed schematic of the op amp is included. Circuit Models and gain improvement techniques for the op amp will be covered as well. Most of the design parameters and specifications are labelled on the diagrams. Lastly, problems

inherently associated with GaAs op amps will be highlighted, such as: low gain, slew rate, offset voltage, etc.

B. GaAs Differential Amplifier Input Gain Stage:

The differential amplifier stage is probably the most critical subcircuit of an operational amplifier. The differential amplifiers' high input resistance and low output resistance renders it quite useful in the design of logic gates, multivibrators, op amps, etc. The GaAs depletion-mode MESFET op amp pictured in Figure 3.1 is the design topology closely followed in the construction of the final amplifier for this study. Specific

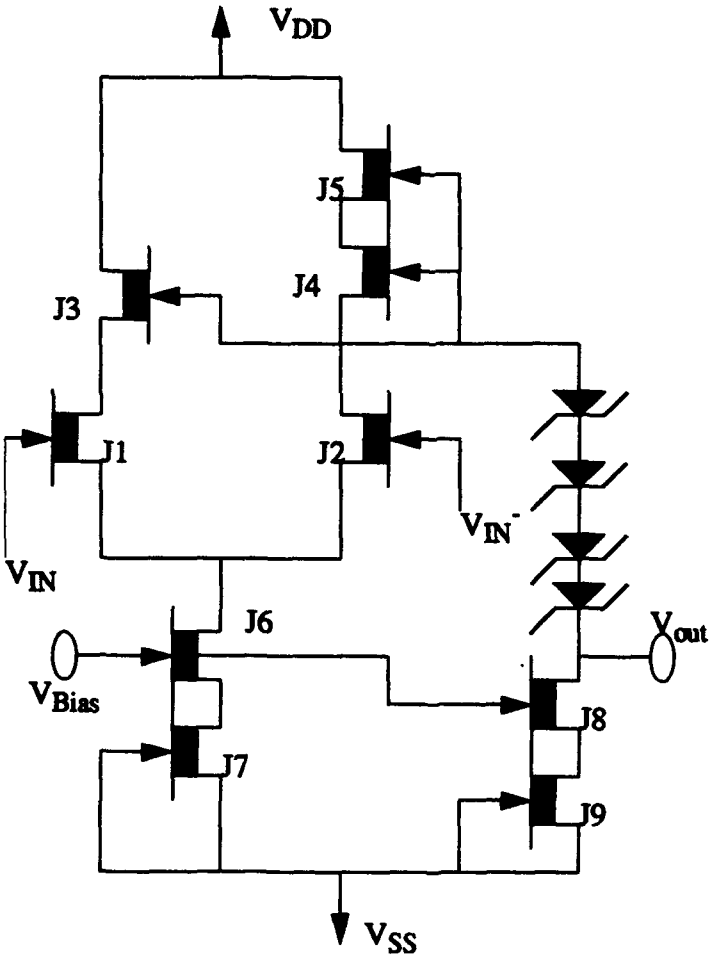


Fig. 3.1 GaAs D-MESFET operational amplifier [4]

dimensions and explanations of all the elements in Figure 3.1 can be reviewed in [4]. This

medium dc gain and bandwidth amplifier is suitable for moderate rate switched-capacitor filters, phase-locked loop, and other medium high speed analog applications. Experimental and simulation results of the above op amp are contained in Table 3.1 below:

TABLE 3.1: Op Amp Performance Parameters [4]

Parameter	Value	Unit
dc gain	40	dB
GBWP	1.3	GHz
Phase margin	80	Deg
Power dissipation	150	mW
Offset voltage	63	mV
Load capacitance	0.4	pf

GaAs op amps possessing improved performance over the one mentioned here have been developed and are available. Such amplifiers can be seen in references [9], [10], [11], and [19]. The performance of the amplifier used in this thesis is not as great as the amplifier in Figure 3.1, still it is more than adequate for composite op amp exploration. Table 5.1 contains the key op amp performance parameters for the op amp designed in this thesis.

In wide bandwidth switching applications, as in high frequency switched-capacitor filter designs, it has been shown that a single-ended single-stage op amp is best [41]. Consider the equivalent circuit model of the single-stage and two-stage op amps in Figure 3.2. In this case, the gain for both models are about the same and is given as:

$$gain = (g_m r_{ds})^2 \qquad \text{(EQ:3.1)}$$

Now, notice that the two-stage amplifier's non-dominant pole location is given by:

$$\left(\frac{-g_{m2}}{C_L}\right) \qquad \text{(EQ:3.2)}$$

and the single-stage amplifier's non-dominant pole location is defined by:

$$\left(\frac{-g_{m2}}{C_{gs2}}\right) \qquad \text{(EQ:3.3)}$$

This is a potentially wider bandwidth than the two-stage op amp. Accordingly, the non-dominant pole plays a key role in the maximum obtainable bandwidth of an op amp

[4]. Additionally, the single-stage op amp is intrinsically much more robust and increases the load capacitance compared to the two-stage model. This makes it more stable [42].

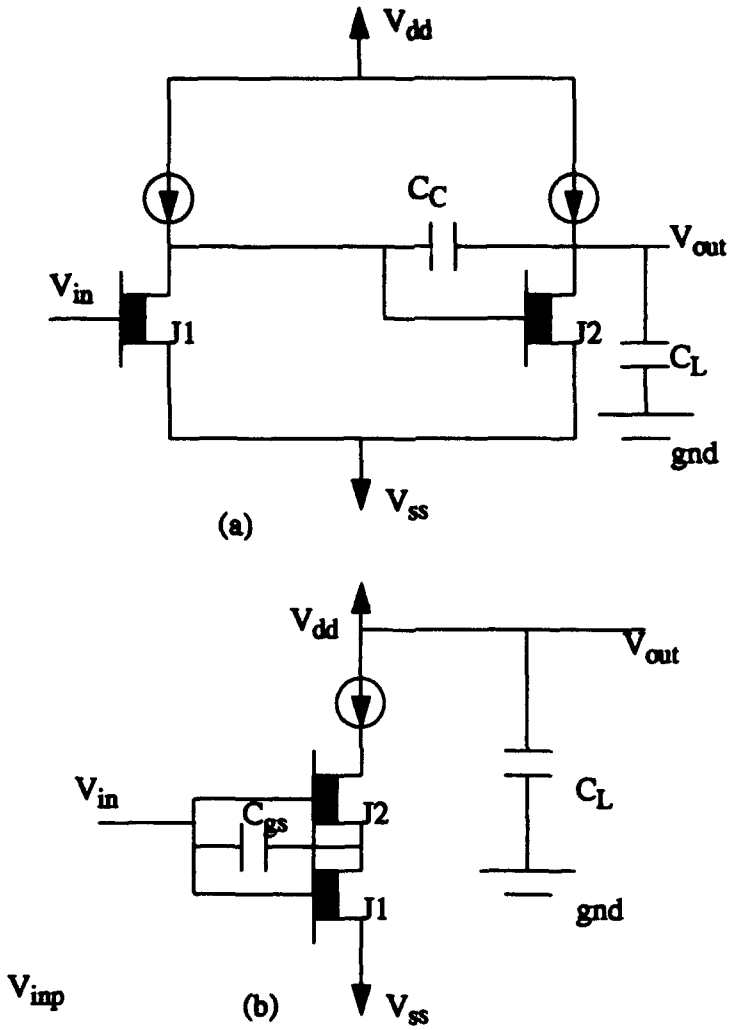


Fig. 3.2 Single-ended equivalent circuit model (a) two-stage (b) single-stage op amp [4]

The discussion above is intended to provide insight on the design models for higher frequency GaAs op amps. However, these models are more complex to implement and will not be employed in the final op amp design.

The final amplifier incorporates forward biased SBDs for level-shifting. Additionally, the high series resistance of the SBDs moderately reduce the amplifier gain. Thus, a careful design strategy must be used when building the level-shifters. The differential amplifier

(diffamp) employs a spliced current source, load transistor, bootstrapping transistor, and positive feedback from the load transistor. Figure 3.3 shows the components of the subcircuit diffamp. The spliced cascode current source is included to provide proper diffamp biasing. Adjusting the bias potential can be accomplished by appropriately altering the gate width. The effects of which were presented in Chapter II. A load transistor and bootstrapping transistor working in tandem provides both gain enhancement and stability.

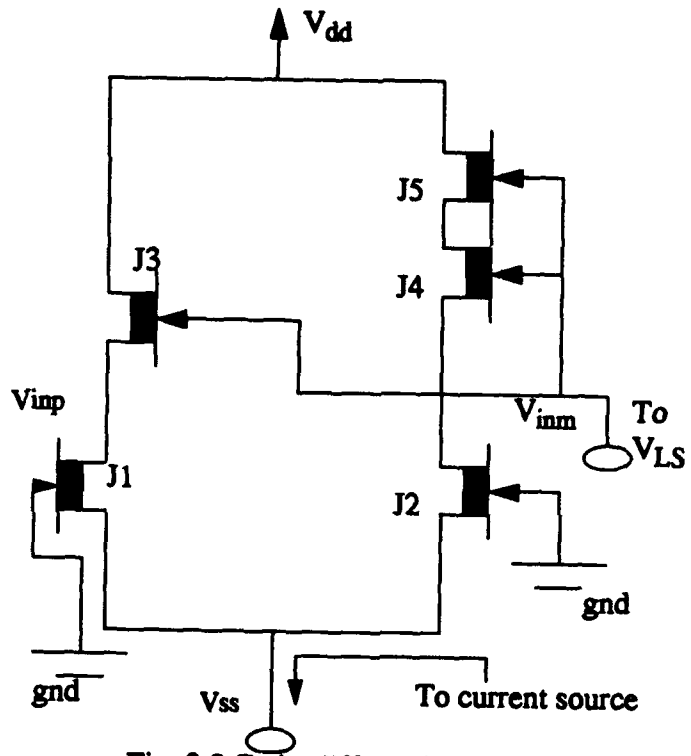


Fig. 3.3 GaAs diffamp input stage

The diffamp uses an active load transistor J4 to maximize gain and the bootstrapping transistor J5 offers both gain enhancement and keeps J4 in the saturation region. This is done through careful selection of the gate width of J5. A positive feedback connection to the depletion transistor J3 at the proper gate width is needed to maintain its forward bias operation. The gate width of J3 is required to be not less than the gate width of the cascode current source transistors J6 and J7 depicted in Figure 3.4. The element dimensions of the

diffamp are based purely on FET design techniques, simulations, and MOSFET equivalent circuit modelling. These element dimensions are given in Table 3.2

TABLE 3.2: diffamp Element Dimensions

FET #	Gate width	Multiplier
1 & 2	2000	1
3	700	1
4	50	1
5	1500	1
6 & 7	15	1
8 & 9	1.0	1
10	110	1
11	2	1
D1 - D3	1.5	15
D4 - D7	1.5	20

FETs J6 - J11 and D1 - D7 are shown in Figure 3.4 below. A GaAs D-FET model with a gate length of 0.8μm was used for all FETs. Also, the diode gate length was set at 0.8μm. The gain for the input diffamp was found to be approximately 21.44.

C. Load Stage and Complete Op Amp:

A series of four forward biased SBDs are used to provide the necessary level-shifting network. The current through these SBDs is kept to a nominal level via the small gate width

load MESFETs. Doing this ensures highest output resistance and improves overall output gain. The complete simulated GaAs D-MESFET schematic is depicted in Figure 3.4.

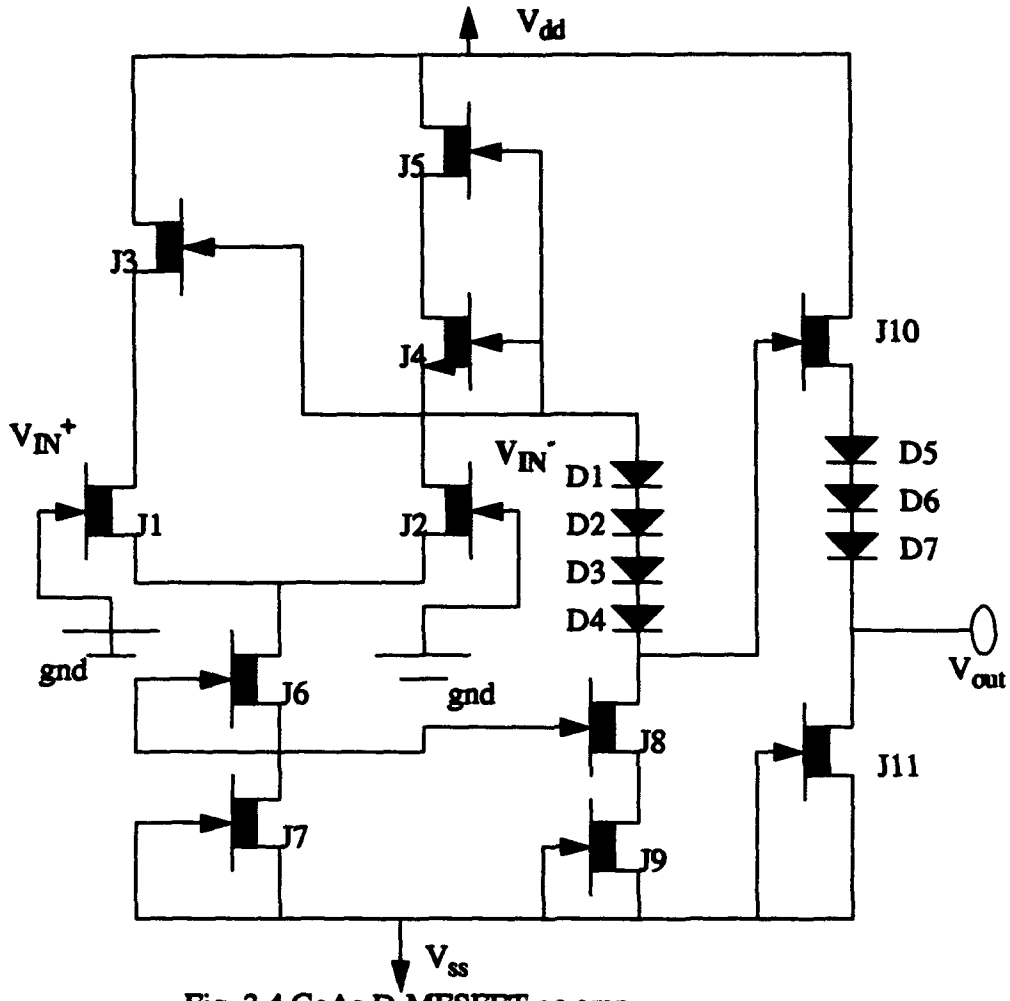


Fig. 3.4 GaAs D-MESFET op amp

The cascode current source consisting of J6 and J7 are employed to increase the output resistance. This was accomplished by following the guidance for gain enhancement techniques for GaAs equivalent models outlined in Chapter II. The optimum gate width for the current source is in Table 3.2 and was determined by several simulation trials. A discernible gain increase was noted when the gate widths of the load FETs were very small, while maintaining the source follower transistor in the saturation mode. Lastly, an external load capacitor of 0.4 or 0.5 pf was used.

D. Op Amp Drawbacks:

The ideal op amp performance characteristics can never be achieved by any non-ideal op amp. Because these performance characteristics have been well documented in other publications, it is not necessary to present all of them here. On-the-other hand, this paragraph will focus on a few drawbacks associated with non-ideal op amps.

The ideal op amp possesses infinite input impedance, zero output impedance, and infinite output voltage gain. However, the non-ideal op amp is hindered by finite dc gain, common-mode rejection ratio, offset voltage, limited bandwidth, slew-rate, finite input impedance, and nonzero output impedance. These topics are pertinent to the overall performance of the op amp. A more exhaustive look at these drawbacks are found in [3], [6], and [28].

1. Finite DC Gain:

As stated above, an ideal op amp possess infinite dc gain, but a non-ideal op amp generally has a finite range of 1000 to more than 1-Meg. for silicon type devices. Yet, for GaAs MESFET op amps, the dc gain range is significantly less, around 100 to 1000.

2. Common-Mode Rejection Ratio:

The common-mode rejection ratio (CMRR) of an op amp is defined by:

$$CMRR = 20log\left(\frac{|A|}{|A_{CM}|}\right) \qquad \text{(EQ:3.4)}$$

where A is the input signal differential gain and A_{CM} is the common-mode gain. The CMRR value is indirectly related to frequency, in that it decreases as the frequency increases. So, in silicon, a typical range for CMRR is 70 to 110 dB for low frequency, and in GaAs, approximately 40 to 60 dB.

3. Offset Voltage:

A general-purpose op amp offset voltage is given as the differential input voltage needed to force the differential output voltage to zero. Thus, when the inputs of a non-ideal

op amp are connected together, a small voltage potential appears at the differential inputs. This voltage potential is amplified at the output. This effect can almost be negated by applying the appropriate offset voltage at the input. It is worth noting that for ideal op amps where the inputs have been connected together, the corresponding output voltage is zero.

4. Effective Bandwidth:

Op amps have reduced available gain across the bandwidth (BW). This reduction in available BW is cause by parasitic capacitances and limited carrier mobility. The problem gets worse as the frequency increases. Also, internally capacitively compensated op amps have a 20 dB roll-off cause by the induced poles from the internal capacitors. Lastly, ideal op amps have infinite gain over the complete BW.

5. Slew-Rate:

The slew-rate (SR) of an op amp indicates the maximum speed at which the output voltage can change. Equation 3.5 is an analytical expression for the SL. The slew-rate is affected by several factors, including component values, input voltage swing, gain, dc supply voltages, etc.

$$SR = \left.\frac{dv_o}{dt}\right|_{max} \qquad \text{(EQ:3.5)}$$

In most cases, the output of the op amp is 1-volt below the positive and negative supply rails.

6. Input and Output impedances:

A general-purpose op amp has finite input impedance in the neighborhood of 10 -20 MΩ. Conversely, the ideal op amp has infinite input impedance.

Briefly, op amps do not exhibit zero output impedance. If this were the case, op amps would operate as an ideal voltage source. Therefore, ICs are frequently designed with buffer stages that have low output resistance in the range of several hundred ohms.

IV. COMPOSITE OPERATIONAL AMPLIFIERS

A. General:

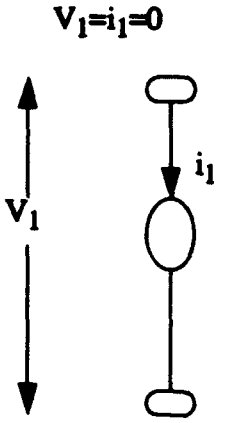
Composite Operational Amplifiers (CNOAs) were developed to extend the effective frequency range of a single op amp, and to reduce some of the drawbacks mentioned in the previous chapter. This is accomplished by using a multiple op amp configuration. In an op amp, the gain bandwidth product and the 3dB frequency are constants. Furthermore, the performance parameters of bandwidth and distortion are not readily controlled when using a single op amp. However, to a certain degree, this has been overcomed and the bandwidth extended through the use of CNOAs.

The CNOA concept was developed in 1981 by S. Michael and W. Mikhael. Their research concentrated on extending the operational frequency of a single op amp and is based on the nullator and norator pairings of some 136 different circuit designs. Each circuit design was evaluated against the performance requirements outlined in [43]. Since CNOAs are not being simulated, only a brief discussion will be devoted to these designs.

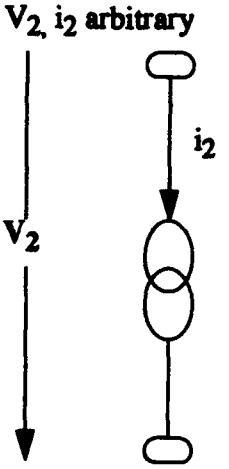
B. Theory Behind CNOAs:

The fundamental operational characteristics of an ideal op amp are infinite input impedance, zero output impedance, and infinite gain. These characteristics can directly be transferred to an idealized model with the use of nullator and norator singular components [1] and [43]. A nullator is a one port device that does not sustain a voltage nor passes a current. On-the-other-hand, a norator is a one port device that sustains an arbitrary voltage

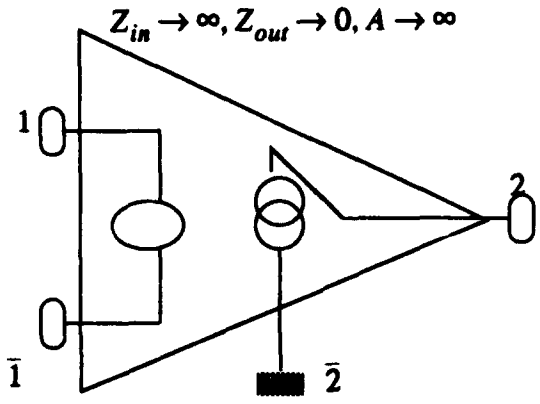
and passes an arbitrary independent current [43] and [45]. Both the nullator and norator along with the hybrid nullor op amp are pictured in figure 4.1.



(a) Nullator



(b) Norator



(c) Nullor op amp (VCVS)

Fig. 4.1 (a) Nullator (b) Norator (c) Nullor op amp

The nullor op amp of figure 4.1c is the re. ılt of applying a nullator-norator analysis technique. From this analysis spurred the creation of 136 CNOAs. The number of CNOAs were reduced to just four, because the others did not meet the performance requirements listed in reference [43]. These four were redesignated as CNOA-1 through CNOA-4, where N=2. The new composite nullor device symbol is very similar to an ordinary single op amp with external input and output terminals.

Equation 4.1 defines the open-loop gain of the single pole op amps used in the C2OAs. These op amps are shown in there composite form at figure 4.2.

$$A_i = \frac{A_{oi}\omega_{Li}}{\omega + s} = \frac{\omega_i}{s + \omega_{Li}}, i = 1or2 \qquad \text{(EQ:4.1)}$$

where A_{oi}, ω_{Li}, and ω_i are the dc open-loop gain, 3dB bandwidth, and the gain bandwidth product (GBWP) of the ith single op amp, respectively. Additionally, the input-output voltage relationship of the C2OA-*i*'s are given below:

$$V_{oi} = V_a A_{ai}(S) - V_b A_{bi}(s), i = 1-4 \qquad \text{(EQ:4.2)}$$

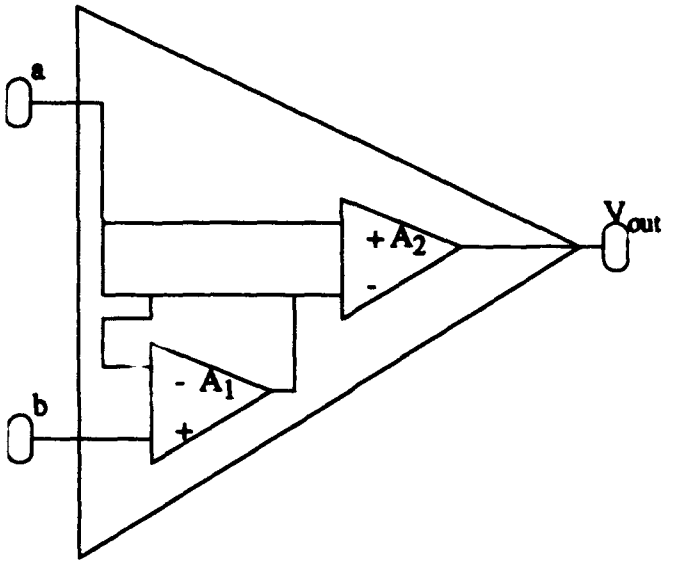


Fig. 4.2 Basic composite op amp symbol

C. Composite Op Amp Topologies:

A brief discussion on each of the four C2OA-*i*'s is presented in the successive paragraphs. To include analytical expressions and conditions for the 3dB frequency, quality factor, gain, and α parameters.

1. C2OA-1:

It has been shown [1] that the open-loop gain for C2OA-1 is defined as indicated in equation 4.3. Also a complete C2OA-1 model is depicted in figure 4.3.

$$V_{01} = V_a \frac{A_2(1+A_1)(1+\alpha)}{A_1+(1+\alpha)} - V_b \frac{A_1 A_2(1+\alpha)}{A_1+(1+\alpha)} \qquad \text{(EQ:4.3)}$$

where α is the internal resistor ratio and is represented in figure 4.3.

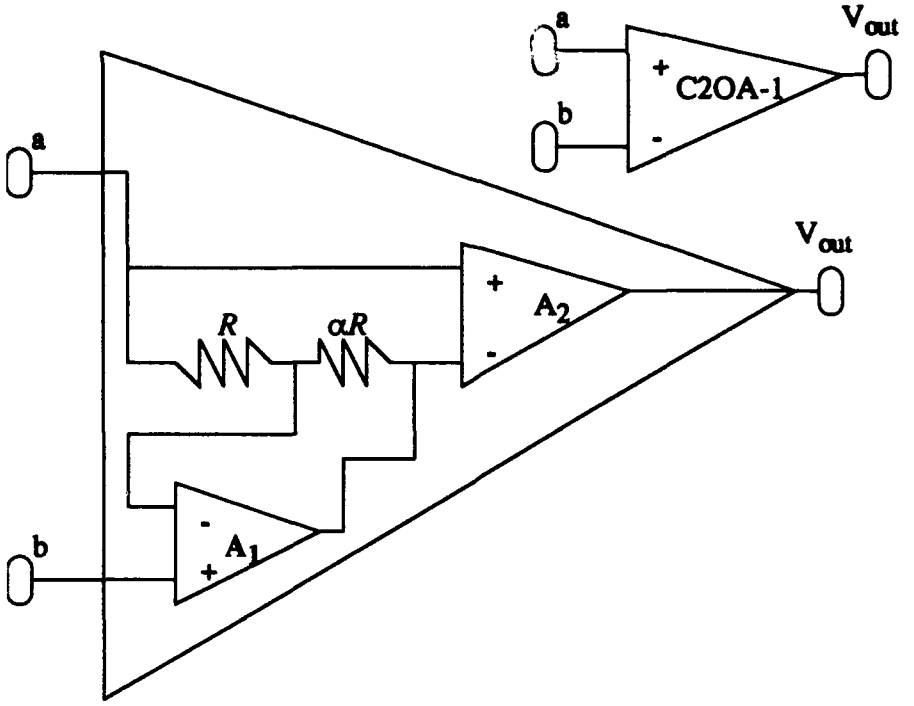


Fig. 4.3 C2OA-1 model

Notice the striking resemblance of the three terminal composite op amp of figure 4.3 to that of a single op amp. Inputs *a* & *b* are the noninverting and inverting terminals respectively. A thorough derivation of the 3dB frequency and the quality factor (Q) for the model above are found in [1] and [2]. An expression for these parameters are given as:

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{1+k}} \qquad \text{(EQ:4.4)}$$

$$Q_p = \frac{(1+\alpha)}{\sqrt{(1+k)}} \sqrt{\frac{\omega_2}{\omega_1}} \qquad \text{(EQ:4.5)}$$

where α is the internal resistor ratio, ω_p is the 3dB frequency, k is the closed-loop gain, and ω_1 & ω_2 are the GBWP for A_1, and A_2 respectively. The system's stability

conditions are validated by applying the Routh-Hurwitz criterion, and the resulting relationship is provided:

$$(1+\alpha) < \frac{1+k}{2} \qquad \text{(EQ:4.6)}$$

2. C2OA-2:

The open-loop voltage gain for C2OA-2 is defined as indicated in equation 4.7. Also, a complete C2OA-2 model is depicted in figure 4.4.

$$V_{o2} = V_a \frac{A_1 A_2 (1+\alpha)}{A_2 + (1+\alpha)} - V_b \frac{A_1 A_2 (1+\alpha)}{A_2 + (1+\alpha)} \qquad \text{(EQ:4.7)}$$

where α is the internal resistor ratio and is represented in figure 4.4.

The 3dB frequency and the Q factor for C2OA-2 are given below:

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{1+k}} \qquad \text{(EQ:4.8)}$$

$$Q_p = \frac{(1+\alpha)}{\sqrt{(1+k)}} \sqrt{\frac{\omega_1}{\omega_2}} \qquad \text{(EQ:4.9)}$$

The Routh-Hurwitz conditions for system stability are given at equation 4.10 below:

$$(1+\alpha) < \frac{1+k}{2} \qquad \text{(EQ:4.10)}$$

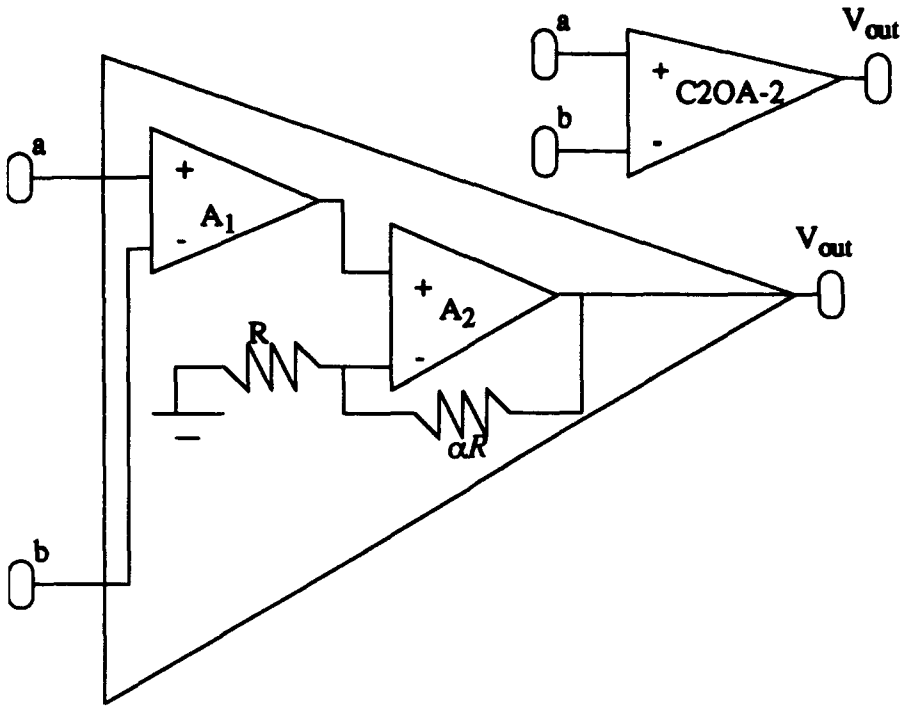


Fig. 4.4 C2OA-2 model

3. C2OA-3:

The open-loop voltage gain for C2OA-3 is defined as indicated in equation 4.11. Also, a complete C2OA-3 model is depicted in figure 4.5.

$$V_{03} = V_a \frac{A_1 A_2}{(1+\alpha)} - V_b \frac{A_2 (1+A_1)}{(1+\alpha)} \qquad \text{(EQ:4.11)}$$

where α is the internal resistor ratio and is represented in figure 4.5.

The 3dB frequency and the Q factor for C2OA-3 are given below:

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{(1+\alpha)\,(1+k)}} \qquad \text{(EQ:4.12)}$$

$$Q_p = \sqrt{\frac{(1+k)\,(1+\alpha)\,\omega_1}{\omega_2}} \qquad \text{(EQ:4.13)}$$

The Routh-Hurwitz conditions for system stability are given at equation 4.14 below:

$$(1+\alpha) > \sqrt{1+k} \qquad \text{(EQ:4.14)}$$

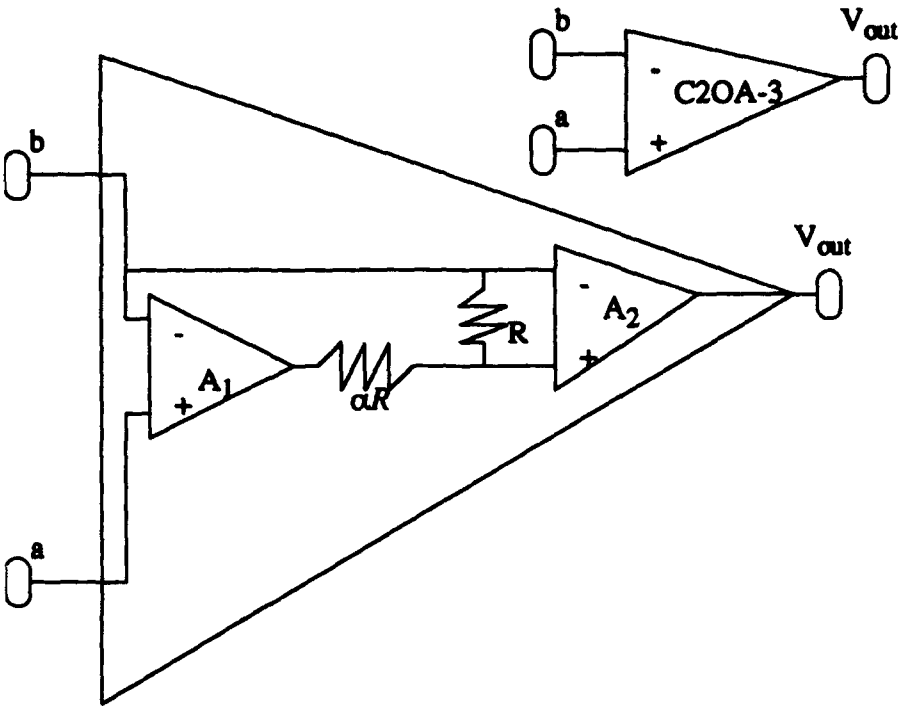


Fig. 4.5 C2OA-3 model

4. C2OA-4

The open-loop voltage gain for C2OA-4 is defined as indicated in equation 4.15. Also, a complete C2OA-4 model is depicted in figure 4.6.

$$V_{04} = V_a \frac{A_2(A_1+\alpha)}{(1+\alpha)} - V_b \frac{A_2[A_1+(1+\alpha)]}{(1+\alpha)} \qquad \text{(EQ:4.15)}$$

where α is the internal resistor ratio and is represented in figure 4.6.

The 3dB frequency and the Q factor for C2OA-4 are given below:

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{(1+\alpha)(1+k)}} \qquad \text{(EQ:4.16)}$$

$$Q_p = \sqrt{\frac{(1+k)\omega_1}{(1+\alpha)\omega_2}} \qquad \text{(EQ:4.17)}$$

The Routh-Hurwitz conditions for system stability are given at equation 4.18 below:

$$(1+\alpha) > 4(1+k) \qquad \text{(EQ:4.18)}$$

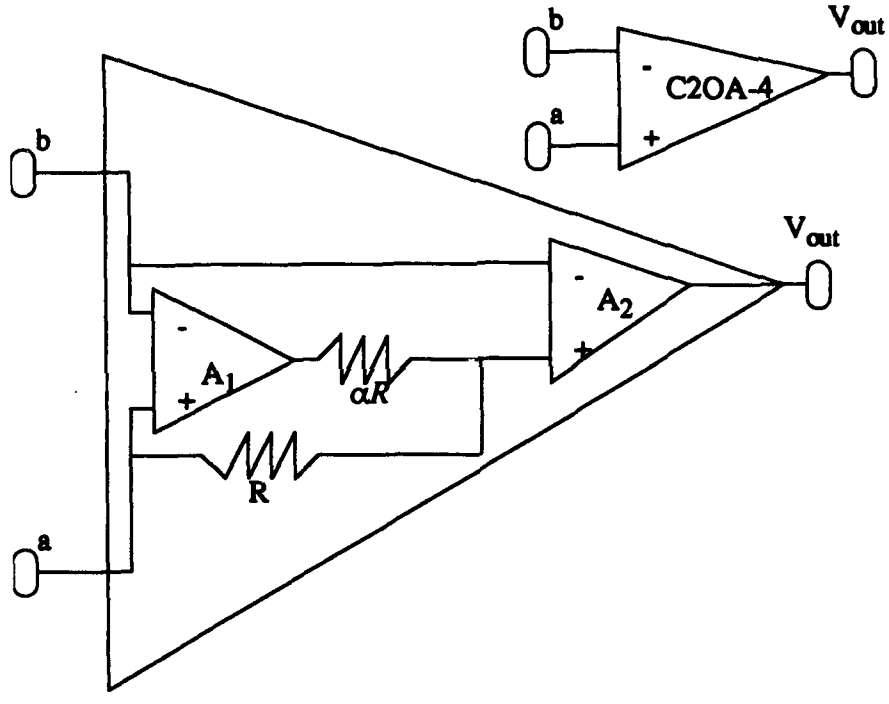


Fig. 4.6 C2OA-4 model

It is worthwhile to point-out that the expressions for ω_p, Q_p, and the Routh-Hurwitz criterion are a function of the parameters α and K. These two parameters also play a key role in implementing a high performance composite op amp. This is described in the

next paragraph. A more detailed and in-depth look at the generation of composite op amps is found at [1], [2], [43], [44], and [45].

D. Determining Appropriate α and K Parameter Values:

In the composite op amp configuration, the designer has much the same control of the closed-loop gain K, as in a single op amp. Once a K value has been chosen, the corresponding 3dB frequency and quality factor can be computed. Likewise, the α parameter is selected by the designer and should be adjusted until the frequency response curve of the composite op amp is maximally flat. Proper and accurate implementation of anyone of the four C2OAs will result in a stable system, as established from the Routh-Hurwitz criterion previously manifested and references [1] and [2].

E. Greater Bandwidth Using C2OAs:

Probably the most significant performance characteristic of the C2OAs is their intrinsic capacity to extend the operational frequency of a given single op amp. In a single op amp configuration, the bandwidth is reduced by a quantity of 1/k. Also, its been documented that cascaded op amps have a bandwidth reduction factor of approximately $\frac{0.66}{\sqrt{K}}$. Alternatively, C2OAs' GBWP can be designed to achieve a smaller shrinkage (as compared to the two previous op amp configurations) roughly $\frac{1}{\sqrt{K}}$ for $Q_p = 0.707$, which is maximally flat [44]. Thus, the composite op amp makes better use of the available bandwidth than the single or cascaded op amp.

F. C2OAs Component Sensitive:

The composite op amp design is less sensitive to fluctuations in both active and passive components [2]. Consider, C2OAs' general transfer function shown below:

$$T(s) = \frac{1 + as}{1 + b_1 s + b_2 s^2} \qquad \text{(EQ:4.19)}$$

where b_1 is defined:

$$b_1 = \frac{1}{\omega_p Q} \qquad \text{(EQ:4.20)}$$

and b_2 is defined:

$$b_2 = \frac{1}{\omega_p^2} \qquad \text{(EQ:4.21)}$$

From the relationships above, it is obvious that neither the *a* nor the *b* coefficients are attained by way of difference equations. This precludes the requirement for single op amps with identical GBWPs, thereby lowering the sensitivity of C2OAs, [2] and [43].

G. Offset Voltages:

All general-purpose op amps have a small differential input voltage between the noninverting and inverting terminals. This differential input voltage is known as the input offset voltage. Its corresponding amplification (caused by gain of the op amp) at the output is called the output offset voltage. If the effects of the offset voltage are not kept to an absolute minimum it could cause a degraded signal at the output. As with single op amps, the composite op amp suffers from differential input offset voltage too.

The composite op amp offers a crafty technique for mitigating the effects of differential input offset voltage. This is accomplished by selecting an op amp A_1, that has a small offset voltage and an op amp A_2, that has a relatively high slew-rate. The benefit of this technique on C2OAs can best be assessed by viewing the definitions for the differential offset voltages listed in Table 4.1.

TABLE 4.1: C2OA Input Offset Voltage

C2OAs	Input Offset Voltages
C2OA-1	$V_{off} = V_{off1} + (V_{off2} / \alpha)$
C2OA-2	$V_{off} = V_{off1} + (V_{off2} / A_1)$
C2OA-3	$V_{off} = V_{off1} + (V_{off2} (1 + \alpha) / A_1)$
C2OA-4	$V_{off} = V_{off1} + (V_{off2} (1 + \alpha) / A_1)$

Observe from Table 4.1 above, the input offset voltage V_{off} is virtually independent of V_{off2} (input offset voltage for op amp A_2), but is heavily dependent on V_{off1} (input offset voltage for op amp A_1). Subsequently, in C2OA-1, as α is made large, the voltage V_{off2} has practically no influence on V_{off}. Moreover, in the other C2OA expressions, V_{off2} is scaled by the value $1/A_1$. Since the open-loop gain is always very high, the effects of V_{off2} is negligible. Neutralizing the adverse effects of the input offset voltages, coupled with the fast slew-rate of A_2, makes the composite op amp design extremely intriguing.

H. C2OA Slew-Rate Considerations:

Most general-purpose op amps are designed to have either a fast slew-rate (SR) or a small offset voltage. Alternatively, a composite op amp makes maximum use of both of these qualities by employing an op amp with a small offset voltage at A_1, and an op amp with a fast SR, wide bandwidth, and fast settling time at A_2. Finally, composite op amps properly designed and implemented vastly out perform any single op amp.

V. SIMULATION RESULTS

A. General:

The GaAs op amp described in Chapter III was simulated in both the open and closed loop modes. The results are presented in this Chapter.

B. Power Supply:

The power supply voltages used in the simulation are selected to accommodate the largest desired input signal swing. For the op amp under test, the values for V_{dd} and V_{ss} were +7.0 and -7.0 volts respectively.

C. Establish Finite Gain:

A closed-loop gain of k=10 was simulated. This was accomplished by selecting R_1= 620Ω and R_f = 6200Ω. This gain is sufficient for testing the design and validating the circuit's functionality.

D. Open-Loop Analysis:

The open-loop circuit simulation was performed many times to verify the validity of the design. Input signals of 10mV and 100mV were applied to the circuits of Figures 5.1 and 5.2 respectively. An input offset voltage of 20mV was applied. A load capacitor of 0.4pF was used in each case. Notice that for each curve the unity gain frequency is approximately 3.0GHz. This unity gain bandwidth is typical of GaAs op amps. The GaAs op amps at references [4], [9], and [10] have similar gain and bandwidth. However, as expected, the low-frequency gain was as measured at 32dB.

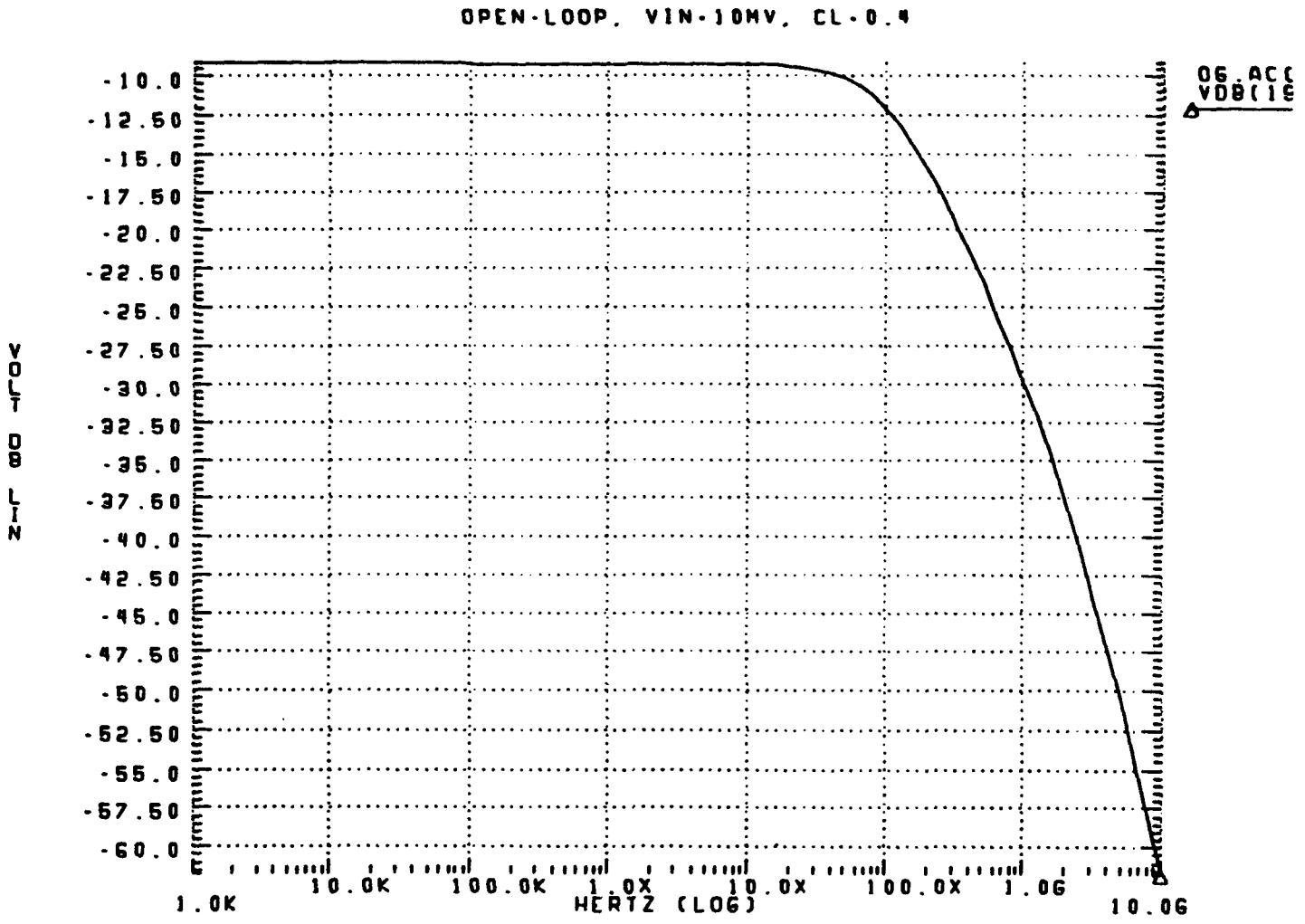


Fig. 5.1 Open-loop response (Vin=10mV)

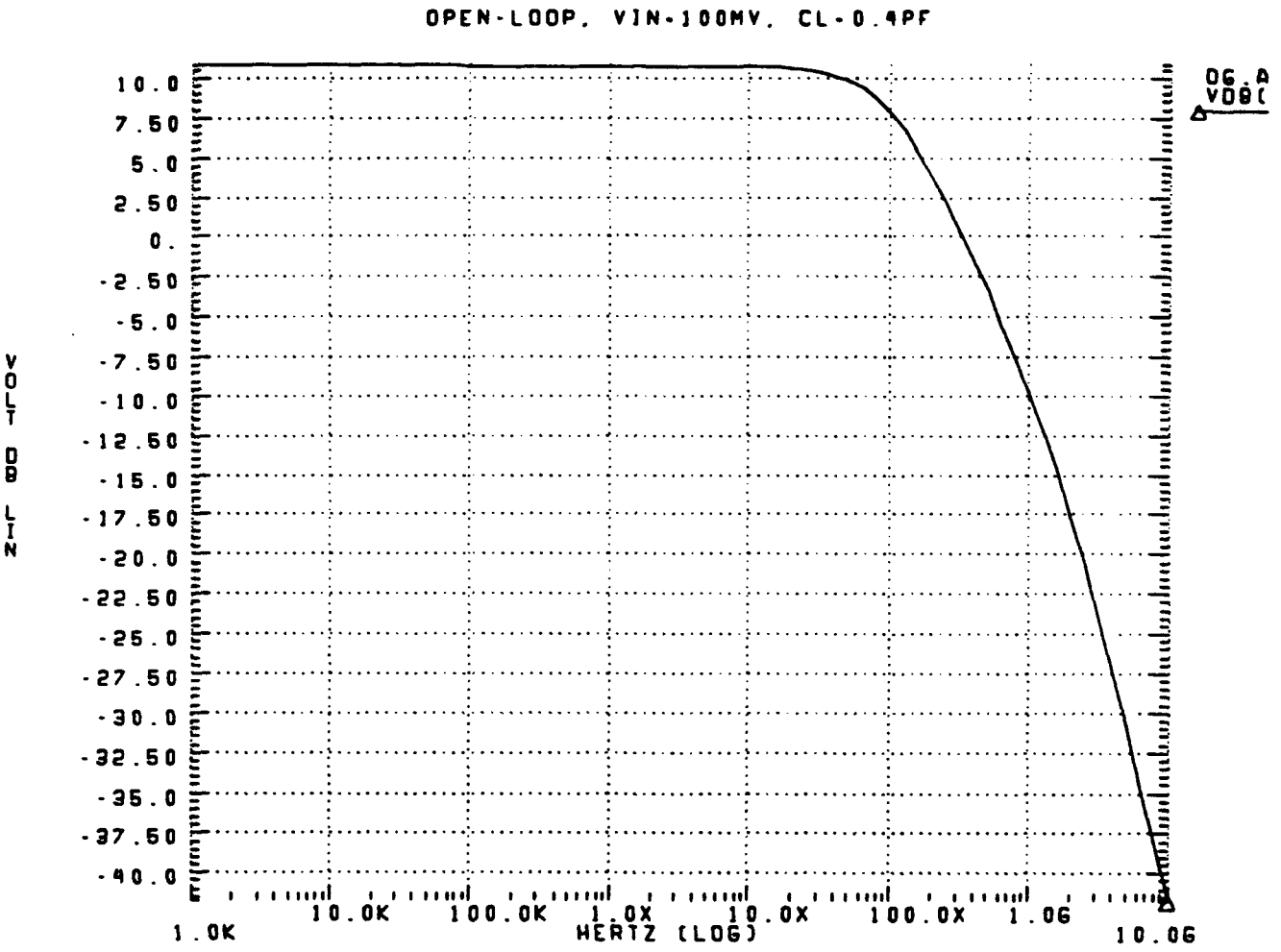


Fig. 5.2 Open-loop gain response (Vin=100mV)

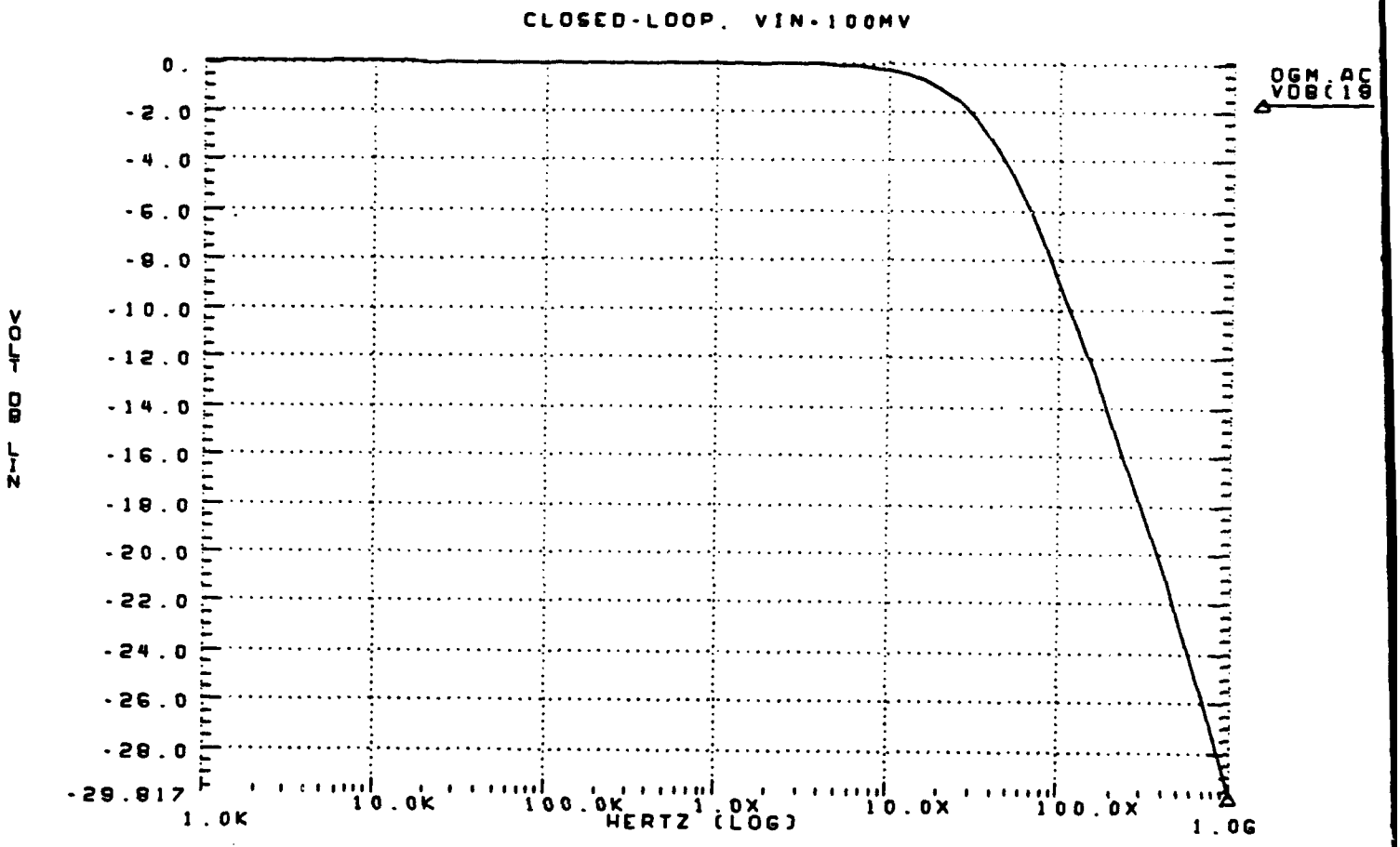


Fig. 5.3 Closed-loop response (K=10)

E. Closed-loop Analysis:

The closed-loop frequency response of the op amp is shown in Figure 5.3, for K=10. The 3dB frequency is approximately 400MHz. This value is better than anticipated, because an op amp's gain-bandwidth is a constant. Again, the power dissipation for this circuit was about 135mW.

TABLE 5.1: Op Amp Performance Parameters

Parameter	Value	Unit
dc gain	32	dB
GBWP	3.0	GHz
Phase margin	135	Deg
Power dissipation	135	mW
Offset voltage	83	mV
Load capacitance	0.4	pf

Finally, Table 5.1 provides a summary of the GaAs op amp's key performance parameters.

VI. CONCLUSIONS AND RECOMMENDATIONS

A. Conclusions:

This research has demonstrated that a general-purpose op amp can be designed using the Vitesse GaAs MESFET process. The performance of the op amp is more than sufficient for composite operational amplifier implementations. The design appears quite stable and should be useful in most high speed applications.

Composite op amps can mitigate the limiting effects of input offset voltage, slew-rate, and reduced operational frequency commonly found in a single op amp. By carefully selecting an op amp with a small input offset voltage for A_1, and an op amp with a high slew-rate for A_2, a composite op amp circuit can be constructed that has significantly improved performance compared to a single op amp.

B. Recommendations for Future Research:

There are many ancillary studies that can be initiated as a result of the findings in this paper. Some of which are listed in the following paragraphs:

1). Design and test the discrete components of the GaAs op amp.

2). Implement the op amp in the design of a composite operational amplifier (CNOAs).

3). Design and fabricate the composite op amp.

4).Determine whether the op amp can be employed in a switched-capacitor network.

6). Revisit the ground level concept of composite operational amplifier generation as it pertains to GaAs MESFETs. In particular, those issues surrounding the low frequency gain and open-loop unity gain frequency.

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